CONTROLLER FOR IN-TRACK LIM PRIMARY

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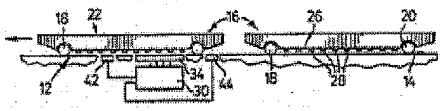
Abstract of **WO9109750**

A controller (30) for a vehicle (16) travelling along a track (12) is provided. The controller includes a pair of sensors (42, 44) disposed along the track which are located on either side of a LIM primary (34). The sensors output signals upon the detection of a vehicle passing thereover. A processor is in communication with the sensors and determines the velocity of the vehicle travelling along the path from the sensor output. A comparator (202) compares the detected velocity of the vehicle with the desired velocity of the vehicle at the vehicle's position along the track as determined by velocity profiles stored in the controller memory (260). A velocity controller (54b) generates velocity correction signals in response to the output of the comparator to operate the LIM primary in a manner to cause the vehicle to assume the desired velocity when the detected velocity is different from the desired velocity. A position controller (56) is also in communication with the processor and the controller memory and overrides the velocity controller when the vehicle is detected as being within a pre-determined distance from a vehicle stopping point along the track as determined by the velocity profile. The position controller generates velocity correction signals to cause the vehicle to stop at the stopping point when the position controller is operational. The velocity correction signals are supplied to a three phase voltage controller (50) connected between the LIM primary and a three phases power supply (32). The controller includes a plurality of switches (61 to 65) operable to connect and disconnect the LIM primary to one of the power supply phases. The controller includes sequencing means (68e) to connect sequentially the LIM to each phase and a delay circuit (68b) to inhibit the sequencing means until the voltage of the power supply reaches a desired level.



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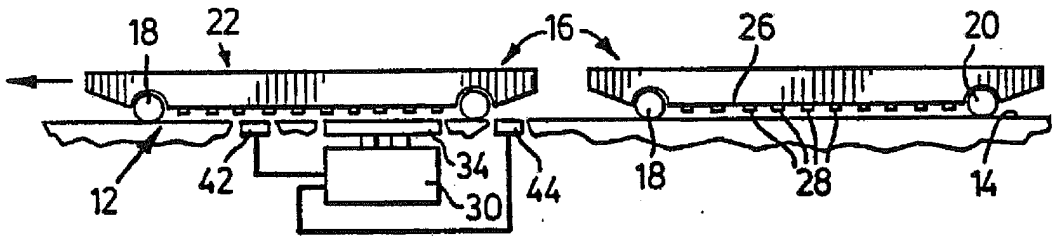

(57) Abstract

A controller (30) for a vehicle (16) travelling along a track (12) is provided. The controller includes a pair of sensors (42, 44) disposed along the track which are located on either side of a LIM primary (34). The sensors output signals upon the detection of a vehicle passing thereover. A processor is in communication with the sensors and determines the velocity of the vehicle travelling along the path from the sensor output. A comparator (202) compares the detected velocity of the vehicle with the desired velocity of the vehicle at the vehicle's position along the track as determined by velocity profiles stored in the controller memory (260). A velocity controller (54b) generates velocity correction signals in response to the output of the comparator to operate the LIM primary in a manner to cause the vehicle to assume the desired velocity when the detected velocity is different from the desired velocity. A position controller (56) is also in communication with the processor and the controller memory and overrides the velocity controller when the vehicle is detected as being within a pre-determined distance from a vehicle stopping point along the track as determined by the velocity profile. The position controller generates velocity correction signals to cause the vehicle to stop at the stopping point when the position controller is operational. The velocity correction signals are supplied to a three phase voltage controller (50) connected between the LIM primary and a three phases power supply (32). The controller includes a plurality of switches (61 to 65) operable to connect and disconnect the LIM primary to one of the power supply phases. The controller includes sequencing means (68e) to connect sequentially the LIM to each phase and a delay circuit (68b) to inhibit the sequencing means until the voltage of the power supply reaches a desired level.

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CONTROLLER FOR IN-TRACK LIM PRIMARY

TECHNICAL FIELD

The present invention relates to a transit system and in particular to a transit system and a controller therefor.

BACKGROUND ART

Linear induction motor (LIM) transit systems are known in the art. Typically, these systems comprise a track supporting a plurality of vehicles which may be interconnected. In some of these systems, LIM secondaries extend along the longitudinal axis of each vehicle and communicate with LIM primaries located at spaced intervals along the track. Sensors for detecting the presence of a vehicle are also disposed along the track at spaced intervals. The sensors communicate with a central processor so that the position of the vehicles along the track can be determined as the vehicles pass between a pair of sensors. The central processor examines the sensor information and determines the speed of the vehicles using various mass and other parameter determining equations.

The detected speed of the vehicles is then compared with the desired speed to determine any differences and appropriate control signals are generated. Controllers located adjacent the LIM primaries operate the LIM primaries so that propulsive forces are applied to the vehicles. The magnitude of the propulsive forces applied to the vehicles are chosen depending on the desired speed of the vehicles as compared with the actual speed of the vehicles so that the vehicles assume their desired speed. However, problems exist in these systems

in that the central processor is required to perform many calculations thereby increasing the necessary information processing time and hence, decreasing the response time of the system.

Moreover, precision velocity and position control of the vehicles in these types of systems is of concern and improvements to these systems are continually being sought.

It is therefore an object of the present invention to provide a novel transit system, a velocity and position controller and a motor voltage controller therefor.

DISCLOSURE OF THE INVENTION

According to one aspect of the present invention there is provided a velocity controller for a vehicle travelling along a path, said controller comprising:

sensing means disposed along said path at spaced intervals for detecting the presence of said vehicle, said sensing means generating output signals as said vehicle moves thereover;

processing means in communication with said sensing means, said processing means receiving said output signals and determining therefrom the velocity of said vehicle along said path;

memory means for storing velocity profiles representing the desired velocity of the vehicle along the path;

comparing means comparing the detected velocity of said vehicle with said velocity profile; and

velocity control means in communication with said comparing means, said velocity control means generating velocity correction signals to operate a linear motor driving said vehicle in a manner so

that said vehicle assumes travel in accordance with said velocity profile when said detected velocity and said desired velocity are different.

According to another aspect of the present invention there is provided a velocity and position controller for controlling the movement of a vehicle along a path comprising:

sensing means disposed along said path at spaced intervals for detecting the presence of said vehicle, said sensing means generating output signals as said vehicle moves thereover;

processing means in communication with said sensing means, said processing means receiving said output signals and determining therefrom the velocity of said vehicle along said path;

memory means for storing at least one velocity profile representing the desired velocity of the vehicle along the path;

comparing means comparing the detected velocity of said vehicle with said velocity profile;

velocity control means in communication with said comparing means, said velocity control means generating velocity correction signals to operate a linear motor driving said vehicle in a manner so that said vehicle assumes travel in accordance with said velocity profile when said detected velocity and said desired velocity are different; and

vehicle position control means in communication with said processing means and said memory means, said position control means being operable when said vehicle is detected as being within a predetermined distance of a stopping point along said path, said position control means overriding said velocity control means upon operation thereof and generating said velocity correction signals to cause said vehicle to stop at said stopping point.

According to yet another aspect of the present invention there is provided a transit system comprising:

a track for supporting a plurality of vehicles, each of said vehicles supporting a linear induction motor secondary and being of capable of travelling along said track;

linear induction motor primaries disposed along said track at spaced intervals to provide thrust to said vehicles to propel said vehicles along said track each of said primaries controlling the motion of a vehicle along a designated zone of said track;

a pair of sensors associated with each of said linear induction motor primaries and located on either side thereof, each of said sensors generating output signals when a vehicle passes thereover;

a motor controller associated with each of said primaries and being in communication with each of said sensors associated with said primary, each of said motor controllers including:

processing means receiving said output signals from said sensors and determining therefrom the velocity of the vehicle travelling along said track within said designated zone;

memory means for storing at least one velocity profile representing the desired velocity of the vehicle along the track;

comparing means comparing the detected direction of travel and speed of said vehicle with said velocity profile; and

velocity control means in communication with said comparing means, said velocity control means generating velocity correction signals to operate said primary to cause said primary to supply thrust to said vehicle, said thrust being of a magnitude and direction so that said vehicle assumes travel along said track in accordance with said velocity profile.

Preferably, the sensing means comprises a pair of spaced sensors, each of the sensors generating a sequence of output signals as a vehicle moves thereover. The sequence of the output signals determines the direction of travel of the vehicle along the path and the rate of change of the sequence determines the speed of the vehicle along the path. The processing means monitors the sequence of output signals and the rate of change thereof to determine the velocity of the vehicle.

It is also preferred that the controller includes jerk-limiting means to prevent the controller from operating the motor primary in a manner which causes the vehicle to jerk due to a substantial increase or decrease in the supplied thrust. Preferably, emergency stop logic is included to cause the vehicle to stop upon detection of sensor failure or upon detection of incorrect vehicle direction travel. It is also preferred that stop detection logic is provided which is operable to generate a velocity correction signal to cause the motor to generate a sufficient thrust to propel a vehicle when the vehicle has stopped in error.

According to yet a further aspect of the present invention there is provided a three phase voltage controller to be connected between a three phase power supply and a linear motor primary comprising:

switching means operable between first and second conditions to connect and disconnect said primary to each phase of said power supply;

control means responsive to control signals for conditioning said switching means between said first and second conditions, said control means including sequencing means operable to condition said switching means to said first condition at a

pre-determined time to connect sequentially said primary to each phase of said supply so that said primary receives a substantially identical supply voltage from each phase of said power supply at the time of connection thereto; and

delay means responsive to said control signals for inhibiting said sequencing means until said supply voltage reaches a desired level.

Preferably, the switching means includes reversing means operable to reverse the connection of two of the three phases of said power supply to said primary. It is also preferred that the switching means is electrically isolated from the control means and that the control means communicates with the switching means via transformers or optical isolation devices.

Preferably, the switching means further includes rectifier circuits for rectifying pulses received from the control means and an inhibitor for disabling the switching means to prevent connection of the primary to the power supply upon receipt of interrupt pulses from the control means.

The present voltage controller provides advantages in that the supply voltage applied to the motor primary can be controlled accurately thereby improving vehicle control in the transit system. Furthermore, the present velocity controller provides advantages in that movement of the vehicle along the path can be controlled with a high degree of accuracy.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Figures 1a, 1b, and 1c are side, front and perspective views respectively of a transit system;

Figure 2 is a side view of a portion of the system illustrated in Figure 1;

Figure 3 is a functional block diagram of a portion of the system illustrated in Figure 1;

Figures 4a to 4d are schematic diagrams of a portion of the system illustrated in Figure 3;

Figure 5 is a functional block diagram representation of the system illustrated in Figure 1;

Figure 6 is a functional block diagram of sensor handling circuitry used in the system illustrated in Figure 1;

Figure 7 is a functional block diagram of a motion control module used in the system illustrated in Figure 1;

Figure 8 is another functional block diagram of a motion control module used in the system illustrated in Figure 1;

Figure 9 is a graph representing the relationship between a velocity correction signal and a power supply delay signal;

Figure 10 is a graph representing the relationship between a gate firing delay angle and a linear induction motor thrust; and

Figure 11 is a representation of a portion of the system illustrated in Figure 1 in operation.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring to Figures 1a to 1c, a transit system is shown and generally indicated by reference numeral 10. The system 10 includes a track 12 having a pair of rails 14. A plurality of vehicles 16 are supported on the rails via their front and rear wheelsets 18,20 respectively. The vehicles 16 can be interconnected to form a train 22 or can be moved along the track 12 as a single independent unit. Each vehicle 16 supports a linear induction motor (LIM) secondary or reaction rail 24 on its undercarriage which extends along the longitudinal axis of the vehicle. Preferably, the reaction rail is designed such as that shown in Applicant's co-pending U.S. Patent application filed on November 8, 1989 and issued Serial Number 432,999, the contents of which are incorporated herein by reference. A steel sensor rail 26 having a plurality of evenly spaced permanent magnetic strips 28 depending therefrom also extends along the length of each vehicle 16, the purpose of which will be described herein.

A plurality of micro-processor based controllers 30 are disposed between the rails 14 of the track at spaced intervals. The controllers are not evenly spaced along the track but rather are located in accordance with the necessary accuracy of vehicle control at a given location along the track. Each of the controllers 30 is connected between a three phase power supply 32 and a LIM primary 34, the LIM primaries of which are also disposed between the rails 14 of the track 12. Each controller 30 is programmed to provide a given motion profile for vehicular travel within a control zone assigned to the LIM primary 34 associated with the controller. The controllers 30 control the supply voltage applied to the LIM primaries 34 so that the vehicle follows the given motion profile during its pass through the control zone assigned to the LIM primary associated with the controller 30, the details of which will also be described herein.

The LIM primaries 34 communicate with the reaction rails 24 secured to the vehicles 16 to provide thrust to the vehicles in a known manner. Since the operation of linear induction motors is well known in the art, details thereof will not be discussed any further herein.

Each of the controllers 30 is also connected to a communications bus 36 which extends to a central or host computer 38. The common link between the host computer 38 and each of the controllers 30 allows the host computer 38 to monitor the operation of the system 10 and record system performance and failures. The host computer 38 also functions to download control information in the form of the motion profiles to each of the controllers 30 upon power up of the system 10. The controllers 30 are connected in parallel to an emergency stop-line 40 which is controlled by a switch (not shown). The emergency stop-line 40 permits emergency shut down of the system 10 in the event of failure.

A pair of sensors 42 and 44 are disposed on either side of each LIM primary 34 and are positioned with respect to the rails 14 so that the sensing rail 26 secured to each vehicle 16 passes thereover as the vehicles 16 move along the track 12. The sensors 42 and 44 are arranged so that one of the sensors always detects the vehicle 16 as it is passing over the LIM primary 34. The sensors 42 and 44 communicate with the controller 30 so that the direction of travel, speed and position of the vehicle 16 passing over the sensors 42,44 can be determined.

Referring now to Figure 2, one of the sensors 42 is better illustrated. Although only one of the sensors 42 is shown, it should be realized that all of the other sensors 42,44 are identical to the

illustrated sensor 42. As can be seen, sensor 42 includes three Hall-Effect detectors 42a spatially oriented to produce a "hexature" like three phase output signal 43 as the magnetic strips 28 depending from the sensing rail 26 successively pass thereover. The detectors 42a are each approximately 1cm in length and the spacing between adjacent detectors 42a is chosen to be approximately 1cm. The spacing between centres of successive of magnetic strips 28 is chosen to be approximately 3cm and the width is chosen to be approximately 1.3cm so that a magnetic strip 28 may only be disposed above one or two of the three detectors 42a of a sensor at a given time. The linear output of each detector 42a is conveyed to a comparator 42b prior to being conveyed to the controller 30. The output signals of the comparators 42b are conveyed to the controller 30 in parallel via an input port 42c and form a changing binary bit-pattern as the magnetic strips 28 pass over each sensor 42. Due to the inter-spacing between the detectors 42a and the magnetic strips 28, the bit-pattern changes for every 0.5cm of travel of the rail 26 and hence, the vehicle 16 over the sensor 42. The provision of the two sensors 42,44 each having three detectors 42a allows the direction of travel as well as the stationary presence of a vehicle 16 to be determined by analyzing the binary value or sequence of output signals 43 from the comparators 42b.

A discriminator circuit 48 is also provided and supplies an interrupt pulse (INT) to the controller 30 when a change of state of one of the sensors 42,44 is detected. This allows idle sensors to be ignored by the controller 30 until a vehicle 16 begins a pass thereover. The discriminator circuit includes a pair of Exclusive-OR (EXOR) gates, each of which receives the binary output signals of one of the sensors. The EXOR gates generate an output signal which changes state each time one of the three signals output by the sensor changes state. An

edge detector is associated with each EXOR gate and produces an interrupt pulse i_n on each transition.

Referring now to Figure 3, a block diagram of one of the controllers 30 is shown. The controller 30 includes power supply switching logic circuitry 50 connected between the three phase power supply 32 and the input terminals 34a of its associated LIM primary 34. A micro-processor based circuit 51 is also included in the controller 30 and comprises control software for performing vehicle position and vehicle velocity control as is represented by blocks 52 and 54. The circuit 51 communicates with the power supply switching logic circuitry 50 and supplies control signals thereto to connect the power supply 32 to the LIM primary 34. The circuit 51 also stores predetermined vehicle operation software as is represented by block 56 as well as sensor handling software as is shown by block 58.

The sensor handling software 58 receives and interprets the output signals generated by the sensors 42 and 44 respectively. Processing and conditioning software represented by block 59 communicates with each of the other software functions and generates the control signals which are conveyed to the switching logic 50. The controller 30 also generates appropriate flags and status signals which are conveyed to the host computer 38 via the communications bus 36 so that the operation and the health of the controller 30 can be monitored. The velocity and position logic functions 52 and 54 along with the pre-determined vehicle operation function 56 are also in communication with the host computer 38 via the communication link 36 and receive operating information therefrom as will be described.

The micro-processor based circuit 51 of the controller 30 includes an Intel 8044 microcontroller which as is well known in the art, combines an 8-bit microprocessor with additional functions for use in real time environments. The circuit 51 also includes resident firmware including RMX-51 Executive firmware which provides a complete operating system and allows multi-tasking capabilities. The 8044 microcontroller is connected to the communication bus 36 via an Intel "BitBus" serial data bus system. An external random access memory (RAM), an external Erasable Programmable Read Only Memory (EPROM), an Intel 8255A Programmable Peripheral Interface (PPI) and an Intel 8254 interval timer are also provided. The Peripheral Interface allows for input/output port expansion and the internal timer provides the timing control for the switching logic function.

Referring now to Figures 4a to 4d, the switching logic circuitry 50 is better illustrated. As can be seen, the circuitry 50 includes five pairs of silicon-controlled rectifiers (SCRs) 61a,61b to 65a,65b, only three pairs 61, 62, 63 or 61, 64, 65 of which operate at a given time. The choice of the three operating pairs of SCRs determines the phase sequence of the three phase power supplied to the LIM primary 34 and hence, the direction of the thrust supplied to the vehicle 16 passing through the control zone associate with the LIM primary 34.

Gate timing circuitry 68 is provided and receives the control signals from the processing and conditioning software 59 in the controller 30. The gate timing circuitry 68 generates the gating signals to operate the proper SCRs at the appropriate time so that the desired amount of propulsive force is supplied to the vehicle 16 via the LIM primary 34.

The gate timing circuitry 68 includes a zero-crossing detector 68a which monitors a 60 Hz A.C. supply voltage applied to a conductor 68b. The supply voltage provided on conductor 68b is the same frequency and is phased with the voltage supplied to the A phase of the three phase power supply 32. A base-period timer 68c communicates with the zero-crossing detector 68a and detects the base period T_b of the 60 Hz A.C. supply voltage. The processing and conditioning software 59 receives the detected base period T_b from the timer 68c and averages the base period T_b over a plurality of cycles of the 60 Hz supply voltage. The processing and conditioning software 59 then divides the averaged base period by six to form a pulse repetition time $T_{b/6}$. The pulse repetition time $T_{b/6}$ is used to sequence the operation of the three pairs of operating SCRs during one cycle of the 60 Hz supply voltage as will be described.

A pulse repetition timer 68d communicates with the processing and conditioning software 59 and stores the value of the pulse repetition time $T_{b/6}$ therein. The pulse repetition timer 68d also conveys an output signal to the shift pin of a shift register 68e. A pulse delay timer 68f receives a delay time t_{fd} generated by the processing and conditioning software 59 and stores the value therein. The delay timer 68f also receives the signal i_{zc} from the zero-crossing detector 68a and provides an output signal to the set pin of a set/reset function 68g and to the pulse repetition timer 68d.

The set/reset function 68g supplies a logic "high" signal to the first register of the shift register 68e upon reception of a pulse from the timer 68f on its set pin. The logic "high" signals supplied to the register 68e by the set/reset function 68g are shifted to successive registers therein upon the reception of shift pulses generated by the

pulse repetition timer 68d. The logic "high" signals shifted through the shift register 68e are outputted via conductors $68h_1$ to $68h_6$ to gating signal conditioning circuitry 70. The output line $68h_2$ is also connected to the reset pin of the set/reset function 68g to cause logic 'low' signals to be supplied to the first register of the shift register 68e after logic 'high' pulses have been received by the first and second registers of the shift register 68e. The delay timer 68f ensures that the output signals passed by the shift register 68e are released to the conductors 68h at the appropriate time as will be described.

The gating signal conditioning circuitry 70 conditions the signals outputted on conductors 68h before they are supplied to the gate of the operating SCRs. The circuitry 70 includes six circuits 72, two 72a,72b of which are associated with conductors $68h_1$ and $68h_4$ and four 72c to 72f of which are associated with conductors $68h_2$,$68h_3$,$68h_5$ and $68h_6$ respectively. The circuits 72a,72b are identical and are each associated with one of the SCRs in SCR pair 61. One of these two circuits 72a is shown in Figure 4d.

The circuit 72a includes a conductor 74 connected to conductor $68h_1$ for receiving the gating pulse outputted by the shift register 68e. The conductor 74 extends to one input of an AND gate 76 while the other input of the AND gate receives an input signal from a frequency generator 78. The output of the AND gate 76 is supplied to the base of a transistor 80. The emitter of the transistor 80 is connected to ground 82 while its collector is connected to a power supply 84 via a relay actuated switch 86 and a transformer primary 88 connected in series. The switch 86 is typically in an open position but moves to a closed condition when an enable signal is received on an enable line GE.

A transformer secondary 90 communicates with the transformer primary 88 and has a rectifier circuit 92 connected across its terminals. The rectifier circuit 92 comprises a diode 92a and a capacitor 92b which convert the AC signals received by the transformer secondary 90 into DC signals before they are supplied to the gate of the SCR 61a. It should be apparent that circuit 72b is identical to circuit 72a but supplies the gating signal to SCR 61b.

The circuits 72c to 72f are also identical to one another and one of the circuits 72c is shown in Figure 4b. Circuits 72c and 72e are associated with SCR pairs 62 and 64 whilst circuits 72d and 72f are associated with the SCR pairs 63 and 65. As is apparent, circuit 72c is associated with one of the SCRs in the pairs of SCRs 62 and 64, namely SCRs 62a and 64a. The circuit 72c includes AND gates 96 and 98 each of which receives the gating signal output by the shift register 68e via conductor $68h_3$. Each AND gate 96,98 also receives a signal from a frequency generator 100 as well as a signal PS from a phase sequence changeover logic circuit 102.

The output signal of the AND gate 96 is supplied to the base of a transistor 104. The emitter of the transistor 104 is connected to ground 82 whilst its collector is connected to a relay actuated switching network 106 via a transformer primary 108. Similarly, the output signal of AND gate 98 is supplied to the base of a transistor 110. The emitter of the transistor 110 is also connected to ground 82 whilst its collector is connected to the switching network 106 via a transformer primary 112. The switching network 106 also receives a control signal from the phase sequence changeover logic 102.

The switching network 106 includes two switches 114a,114b, each of which is connected to one of the transformer primaries 108,112 respectively at one of its terminals. The other terminals of each switch are interconnected and extend to the power supply 84 via the switch 86. The switches 114 are operated between open and closed positions by a relay 118 that is energized by the phase sequence changeover logic 102. The switches 114a,114b are maintained in opposite positions so that only one of the two transformer primaries 108, 112 is connected to the power supply 84 at a given time when the switch 86 is enabled.

A transformer secondary 120a,120b is associated with each transformer primary. A rectifier circuit 122a,122b comprising a diode and a capacitor is connected across the terminals of each transformer secondary 120 and similarly functions to convert the AC signals received by the transformer secondary into DC signals before they are supplied to the gate of the SCR. It should be apparent that transformer 122a supplies a gating signal to SCR 62a while transformer 122b supplies a gating signal to SCR 64a. It should also be apparent that circuit 72d provides gating signals to SCRs 63a and 65a in response to signals provided on conductors $68h_5$, that circuit 72e provides gating signals to SCRs 62b and 64b in response to signals provided on conductors $68h_6$ and that circuit 72f provides gating signals to SCRs 63b and 65b in response to signals received on conductors $68h_2$.

Referring now to Figure 5, one of the controllers 30 is better illustrated. As can be seen, the sensor handling software 58 receives the output signals generated by the sensors 42,44 along with the interrupt signals i_x generated by the discriminator circuit 48. The

sensor handling software 58 interprets the sensor information to produce useful vehicle position and direction information.

The sensor handling software 58 is further illustrated in Figure 6. As can be seen, the changing bit-pattern received from the operating sensor is applied to a sensor verification function 58a. Since the correct bit-pattern which should be output by the sensors as a vehicle 16 passes over the sensors is known, the proper operation of the sensors can be determined. This is done by comparing the bit-pattern output by the operating sensor with the proper known bit-pattern sequence. The verification function 58a performs this task and outputs a sensor failure flag Sf1,Sf2 if one or both sensors 42,44 is detected as malfunctioning.

A sensor handover manager function 58b also receives the output of the sensors 42,44. This function monitors the 'active' sensor and manages the handover between the sensors 42,44 as the vehicle 16 passes over the pair of sensors 42,44 so that accurate vehicle position can be maintained. A direction detector 58c is in communication with the manager 58b and compares successive bit-patterns generated by the operating sensor to detect the direction of travel of the vehicle along the track 12. The direction detector 58c in turn generates a direction travel flag DT indicating the direction of travel of the vehicle 16 over the sensor. A direction change detector function 58d also communicates with the manager 58b and produces a direction change flag DC when a change in direction of a vehicle 16 passing over a sensor is detected.

A position counter 58c within the sensor handling software 58 increments or decrements its count upon receipt of each 3-bit pattern

received from the operating sensor depending on the direction of travel of the vehicle and records the time corresponding to the new position of the vehicle. Since the sensors 42,44 and sensing rails 26 are arranged to output a different 3-bit pattern upon every 0.5cm of travel of a vehicle, position control of the vehicle can be maintained with an accuracy of up to 0.5cm. The output flag P_f of the counter 58e is conveyed to an update recorder 58f which records the time T between successive updates of the position counter. The sensor handling software 58 is synchronized through the basic sensor signals and thus, when the vehicle 16 is passing over the sensors at a high speed and the sensor output changes frequently, the sensor handling function is at its busiest.

The signals generated by the sensor handling software 58 are firstly conveyed to a buffer 200. Thereafter, the sensor failure flags Sf1, Sf2 if generated, are conveyed to the host computer 38 via the communication bus 36 so that the failure can be recorded. The sensor failure flags are also conveyed to emergency stop logic 226. The direction change flag DC if generated, is conveyed to gate inhibit logic 229.

At periodic intervals of approximately 50msecs, thrust control logic is executed which samples the position count P_f, direction travel flag DT and time flag T from the buffer 200 and conveys the sampled values to a velocity calculator 54a forming part of the velocity logic 54. The task firstly examines the vehicle position to determine if the vehicle position is within the bounds of the control zone selected for the LIM primary as determined by selected vehicle operation information. If the vehicle is detected as being within the control zone assigned to the LIM primary, the position count P_f, direction travel DT

and time flags T are again sampled from the buffer. From the consecutive samples of vehicle position, direction and time flags, the velocity calculator 54a determines the time taken between successive position count updates and the distance travelled by a vehicle between each position count update (0.5cm). Since the direction of travel of the vehicle 16 is known from the value of the flag DT, the velocity of the vehicle 16 passing over the operating sensor is determined from this information. The determined velocity V_f generated by the calculator 54a is then applied to a velocity controller 54b.

The velocity controller 54b is better illustrated in Figure 7 and includes a subtracter 202 which receives the detected velocity V_f of the vehicle 16 as well as a desired vehicle velocity V_d from a motion profile stored in logic 56. The velocity V_d represents the desired velocity of the vehicle at the vehicles position along the track 12. The difference e between the detected velocity V_f and the desired velocity V_d of the vehicle at position P_f along the track that is determined by the subtracter 202 is applied to a pair of scaling functions 204 and 206.

The scaling function 204 calculates the 'proportional' component e_p of the desired velocity control signal by scaling the difference e by a constant K_p representing the proportional gain for vehicle velocity control. The scaling function 206 calculates the 'integral' component e_i of the desired velocity control signal by scaling the difference e by a constant k_i representing the integral gain for vehicle velocity control and adding to the scaled result, the previously calculated 'integral' component e_i generated by function 206. The constants k_p and k_i are experimentally determined for a particular combination of vehicle mass, drag and motor thrust and are selected so that optimal stability and response is achieved. The gain constants k_i and k_p (proportional

gain) are stored in the controller memory and are received from the host computer 38 upon power up of the system 10.

The output of each scaling functions 204 and 206 respectively is applied to an adder 208 which in turn forms a velocity correction signal C_v. The velocity correction signal C_v is then applied to a loop selector 220 forming part of the processing and conditioning software 59. The loop selector 220 also receives control signals from the position logic 52 and the position count P_f from the buffer 200. The loop selector 220 is typically in communication with the velocity logic 54 and is operable to pass the correction signal C_v to deadstart logic 222. The deadstart logic 222 allows the correction signal C_v to pass unless the vehicle 16 has stopped in a position along the track wherein it was not intended to stop. If this occurs, the correction signal C_v is set to a value C_{start} stored in the controller RAM so that the vehicle 16 can be started from its stopped position. This is achieved by setting the correction signal to the value C_{start} which will ensure that the LIM primary 34 applies sufficient thrust to the vehicle 16 so that it begins moving along the track in the desired direction.

The deadstart logic 222 conveys the correction signal C_v to a jerk-limiter 224 which in turn passes the signal to the emergency stop logic 226. The jerk-limiter monitors the correction signal C_v and compares its value with the previously formed correction signal. The difference between the signals which represents the rate of change of the correction signal, is then compared with a pre-determined constant J stored in the controller memory. If the rate of change of the correction signal generated by the controller 54b is less than the constant J, the correction signal C_v is passed to the emergency stop logic 226. However, if the rate of change of the correction signal

exceeds the constant J, the correction signal is modified to the limiting rate set by the value of the constant. The modified correction signal is then applied to the emergency logic 226. This ensures that the vehicle 16 is not supplied with a thrust which will cause it to jerk violently due to a sudden increase or decrease in velocity.

The emergency stop logic 226 receives the sensor failure flags Sf1 and Sf2 and the direction travel flag DT from the buffer 200 and other health and failure flags from other functions in the controller 30 in addition to the correction signal C_v. In proper operation of the system 10, the logic 226 allows the correction signal received from the logic 224 to pass. However, if the emergency stop line 40 or another failure in the system 10 is detected which requires emergency stopping of the vehicle or vehicles 16, the direction travel flag DT is checked by the emergency stop logic 226. Thereafter, the correction signal is set to a value C_{es} and a control signal is conveyed to the phase sequence select logic 102 in circuits 72c and 72d so that the direction of thrust supplied by the LIM will be opposite to that of the vehicle travel. The retarding thrust generated by the LIM is maintained until the sensor handling function 58 generates a direction change flag DC. The direction change flag DC is then conveyed to the gate inhibit logic 229. At that time, the gate inhibit logic 229 generates an inhibit signal thereby preventing switch 86 from closing so that the LIM primary 34 is isolated from the power supply 32. The emergency stop logic 226 also functions to stop automatically a vehicle 16 which appears to be travelling in the wrong direction over a sensor and when a sensor failure is detected in the above-described manner.

Before the LIM primary 34 is energized, the correction signal C_v or C_{es} output by the emergency stop logic 226 is firstly conveyed to

a linearizer or phase delay convertor 228. The linearizer 228 in turn examines the magnitude and polarity of the correction signal and selects a timing or phase delay signal associated with the correction signal. The linearizer 228 is able to select one of 127 different delay times t_{fd} for a correction signal, the selected delay time being dependent on the magnitude and polarity of the correction signal. The linear approximation used to select the delay time t_{fd} for a given correction signal is illustrated in Figure 9 by way of the dotted line. The delay time t_{fd} is in turn conveyed to the gate timing logic so that the LIM primary 34 can be connected to the power supply 32 at the correct time. This ensures that the vehicle 16 passing over the controller 30 is supplied with a thrust which causes the vehicle to assume the desired velocity V_d or a velocity associated with the correction signal supplied to the linearizer. The relationship between the LIM thrust and the firing delay angle of an SCR (determined by the time delay t_{fd} is shown in Figure 10.

A position controller 240 forming the position logic 52 is also in communication with the buffer 200 and receives the output flag P_f generated by the position counter. The position controller 240 also receives the detected velocity V_f of the vehicle 16 from the velocity calculator 54a. The position controller 240 includes a subtracter 242 which determines the difference q between the detected position of the vehicle 16 along the track 12 and the position along the track at which the vehicle 16 is required to stop. The position controller overrides the velocity controller 54b when the vehicle approaches a pre-determined distance P_{zone} from a vehicle stopping point P_{stop} in the control zone assigned to the LIM primary 34. The stopping point and distance values are stored in a memory 243 and are received from the host computer 38 upon power up of the system. This is accomplished by

providing a control signal to the loop detector 220 causing it to disconnect the velocity controller 54b from the deadstart logic 222 and connect the position controller 240 to the deadstart logic 222.

The detected difference q between the position of the vehicle and the position of the stopping point P_{stop} that is generated by the subtracter 242 is conveyed to a pair of scaling functions 244 and 246. The scaling function 246 calculates the 'proportional' component q_p of the desired position control signal by scaling the difference q by a constant j_p representing the proportional gain for vehicle position control. The scaling function 244 calculates the 'integral' component q_i of the desired vehicle control signal by scaling the difference q by a constant j_i representing the integral gain for vehicle position control and adding to the scaled result, the previously calculated 'integral' component q_i generated by function 244. However, the function 244 also receives the position count P_f and automatically resets the value of the integral component q_i to zero if the position count changes.

The detected velocity V_f is conveyed to a third scaling function 249 which calculates the 'derivative' component of the position control signal by scaling the detected velocity V_f by a constant j_d representing the derivative gain (damping) for position control. The gain constants J_i, j_p and j_d are stored in the controller memory and are received from the host computer 38 upon power up of the system 10. The constants are also experimentally determined for a particular combination of vehicle mass, drag and motor thrust and are selected so that optimal stability and response is achieved. The output q_i and q_p of the functions 244 and 246 are added via a summing block 248. The summing block 248 also receives the output signal q_d from the scaling

function 249 and subtracts this value from the other two values to form the correction signal.

The correction signal output of the summing block 248 is conveyed to the loop selector 220 wherein it is passed to the deadstart logic 222 as a correction signal. The correction signal is conditioned if necessary in the same manner as previously described. Thus, the correction signal generated by the position controller 240, results in a time delay signal t_{fd} being generated which in turn causes the LIM primary 34 to be energized with the supply voltage at the appropriate time so that the vehicle 16 comes to a stop at the stop position P_{stop}. When the vehicle 16 is not required to stop during a motion profile, the position controller 240 is inoperative.

The pre-determined vehicle operation logic 56 includes a memory 260 for storing a plurality of motion profiles representing the desired velocity of the vehicle for positions of the vehicle along the track within the control zone that are controlled by the LIM primary 34 associated with the controller 30. The motion profiles are precalculated according to the requirements and constraints of the system 10 and are downloaded as a table of data to each of the controllers 30 from the host computer 38 upon power up of the system 10. In the preferred embodiment, a single profile may contain up to 10 points, a point consisting of two numerical values i.e. demand or desired velocity V_d and its associated position P_f along the track. The memory may contain up to 8 motion profiles at a given time and is conditioned to access one motion profile table in response to commands received from the host computer 38 via a table selector 262.

A monitor task 264 is also included in the processing and conditioning software 59 which performs periodic checks on certain external signals and keeps a health status report of the system 10. The monitor function measures the time the controller 30 spends prepared for activity prior to controlling a vehicle 16 and generates a time mode indicator TO1 if this time exceeds a preset limit. The task also measures the time the power supply 50 switching logic is operating to connect to the three phase power supply the LIM primary 34 and sets a time mode indicator TO2 if this time exceeds a preset limit. The monitor task also verifies external input which contains various over temperature indicator signals LT2 and the emergency stop command ES. Since the monitor task function communicates with all aspects of the controller 30, the health status each of the controllers 30 in the entire system 10 is maintained. The health status of each controller 30 is also conveyed to the host computer 38 via the communication bus 36 so that the health of the overall system can be monitored.

The operation of the system 10 will now be described. Upon power up of the system 10, the host computer 38 downloads the various motion profiles, vehicle stopping points and zones and the constants for use by the velocity and position controllers to each of the controllers 30 disposed along the track via the communications bus 36. Once the profiles have been received and stored in the controllers 30, the host computer 38 provides selection signals to the controllers 30 so that the desired motion profile is selected by each controller 30 via the selector 262. Thereafter, the system 10 becomes operational.

The controllers 30 disposed along the track 12 remain inactive until a vehicle 16 has been detected over one of the sensors 42,44 associated therewith. When a vehicle 16 travels along the track, and

the sensor rail 26 passes over a sensor 42,44, the sensor begins to output the "hexature" signals 43. Once the change of state of the sensor has been detected, the discriminator circuit 48 enables the controller 30 so that analysis of the sensor output signals can be performed.

As mentioned previously, the velocity calculator 54a which samples the output of the sensor handling logic 58 via the buffer 200 at regular intervals determines the velocity V_f of the vehicle 16 passing over the sensor. The controller 30 then compares the detected velocity V_f of the vehicle 16 at position P_f along the track with the desired velocity V_d of the vehicle at the same position as determined by the selected motion profile. If the vehicle at its detected position along the track is not travelling in the proper direction or speed as compared with that listed in the motion profile, a correction signal is generated by the velocity controller 54b and is conveyed to the linearizer 228 via the loop selector 220 after being conditioned via the deadstart logic 222, the jerk-limiting logic 224 and the emergency stop logic 226 in the manner previously described.

Alternatively, if the loop selector 220 is conditioned to connect the position controller 240 to the dead start logic 222 due to the proximity of the vehicle to a stopping point within the control zone of the LIM primary, the correction signal is generated by the position controller and is conveyed to the linearizer 228 in the manner previously described.

When the LIM primary 34 is to be energized to alter the motion of the vehicle 16, the controller 30 operates the switching logic 50 to connect the LIM primary 34 to the three phase power supply 32. The

LIM primary 34 then provides the desired thrust to the vehicle 16 so that the vehicle assumes travel in the desired manner.

In particular, when the system 10 is powered up and the 60 Hz A.C. voltage is applied to the conductor 68b, the base period T_b of the A.C. line voltage is determined by the zero-crossing detector 68a and the base-period timer 68c. This is achieved by the base period timer 68c which measures the time taken between successive positive zero-crossings detected by the zero-crossing detector 68a. This time is then conveyed to the processing and conditioning function 59 at block 266 of Figure 5. The function 59 in turn averages the base period time over several cycles of the AC voltage and divides the averaged value by six to yield the pulse repetition rate $T_{b/6}$. The pulse repetition rate is then conveyed to the pulse repetition timer 68d which uses the calculated pulse repetition rate to generate six substantially evenly time spaced pulses between successive positive zero-crossings of the A.C. voltage.

Once this is done, the time delay t_{fd} determined by the linearizer 228 (in response to the received velocity or position correction signal) which corresponds to the required SCR delay angle is conveyed to the pulse delay timer 68f and stored therein. When a positive zero-crossing is detected by the detector 68a, the signal i_{zc} is generated and conveyed to the delay timer 68f. The delay timer 68f begins a count upon reception of the pulse i_{zc} until the delay time t_{fd} is reached. Once the count reaches a value equal to the delay time t_{fd}, a set pulse is applied to the set/reset function 68g and to the pulse repetition timer 68d. The set/reset function 68g in turn supplies a logic "high" to the load pin of the shift register 68e causing the first register therein to store a logic "high". The logic "high" is conveyed along conductor $68h_1$ to operate SCR 61a as will be described.

Once the pulse repetition timer receives the logic "high" from the set/reset function 68g, the timer 68d begins to output the six pulses to the shift pin of the shift register 68e. The first shift pulse causes the logic "high" placed in the first register to shift to the second register. The set/reset function 68g which remains in the set mode, maintains a logic "high" on the load pin so that the first register is supplied with another logic "high". This causes the first two registers of shift register 68e to store logic "highs". The second register applies the logic "high" to the conductor $68h_2$ which causes SCR 63b to operate. The logic "high" is also applied to the reset pin of the set/reset function which causes the function 68g to reset so that the load pin is supplied with a logic "low" during additional shifts of the shift register 68e in response to output pulses generated by the pulse repetition timer 68d. Thus, the logic "high" on conductor $68h_1$ remains for a time equal to $2*T_{b/6}$. This ensures that the SCR 61a is operated for a 120^0 duration so that the SCR 61a conducts until commutation. The second shift pulse outputted by the pulse repetition timer 68d causes the contents of the first and second registers to down shift so that logic "high" values are stored in the second and third registers. When the third register receives the logic "high" from the second register, the logic "high" is applied to conductor $68h_3$ which causes SCR 62a to operate.

Subsequent pulses released by the pulse repetition timer 68d shift the second and third logic "highs" to the third and fourth, fourth and fifth and fifth and sixth registers before the cycle is repeated again upon reception of the next positive zero-crossing of the 60Hz supply voltage. The two bit wide pulses applied to each conductor 68h correspond to a gating signal duration of 120^0 and are conveyed to the gate signal conditioning circuitry 70 before the SCRs are operated. The circuitry 70 is arranged to direct the shift register output logic

"high" values to the gates of the positive phase SCR pairs 61,62,63 if the correction signal has a positive polarity and the negative phase SCR pairs 61,64,65 if the correction signal has a negative polarity. A positive polarity correction signal corresponds to a forward thrust and a negative polarity correction signal corresponds to a reverse thrust.

The phase sequence changeover logic 102 is included to ensure that when a transition from positive to negative phase sequence occurs, sufficient time is allowed for one of the set of SCRs to cease conducting before the other set is gated on. The phase sequence changeover logic 102 also monitors the polarity of the correction signal and operates the switching network 106 and the proper AND gates 96,98 so that the proper SCRs are operated.

When the pulses are shifted along the register of the shift register 68e, a logic "high" value corresponding to $2^* T_{b/6}$ is applied successively to each conductor $68h_1$ to $68h_6$. Due to the wiring convention of conductors 68h to the SCRs 61 to 65 via the circuits 72, the SCRs are operated in sequence 61a, 63b, 62a, 61b, 63a and 62b during one cycle of the A.C. supply voltage for forward thrust and 61a, 64b, 65a, 61b, 64a and 65b for reverse thrust. Thus, when the correction signal has a positive polarity to cause a forward thrust to be applied to the vehicle 16 via the LIM primary 34, the shift register output pulse applied to conductor $68h_1$ is conveyed to the AND gate 76 via conductor 74. The gate 76 which also receives an input from the frequency generator 78 provides a pulse to the base of transistor 82 causing it to conduct. When this occurs, current flows from the supply 84 to the ground 82 via the switch 86, the transformer primary 88 and the transistor 80. The current flow through transformer 88 energizes the transformer secondary 90 causing current to flow therein. The

rectifier circuit 92 rectifies the AC pulse before it is supplied to the gate of the SCR 61a. The DC pulse received on the SCR gate causes the SCR 61a to conduct thereby connecting phase A of the power supply 32 to the LIM primary 34.

After the first shift of the register, a logic "high" is also applied to conductor $68h_2$ which provides a pulse to SCR 63b via circuit 72f. In particular, the pulse from conductor $68h_2$ is applied to AND gates 96 and 98 which also receive logic "high" values from the frequency generator 100. However, since the thrust to be supplied to the vehicle 16 is positive in this example, the phase changeover logic 102 provides a logic "high" pulse only to AND gate 96. The logic "high" pulse from logic 102 is also conveyed to coil 118 to connect switch 114a to the power supply 84. The operation of AND gate 96 provides a logic "high" to the base of transistor 104 causing it to conduct. When this occurs, current flows from the supply 84 to the ground 82 thereby energizing the transformer primary 108 and in turn the transformer secondary 120a. This causes a logic high to be applied to the gate of SCR 63b. When a negative thrust is to be supplied to the vehicle, AND gate 98 is operated and switch 114b is connected to the power supply 84 to energize SCR 64b.

Similarly, when conductors $68h_3$, $68h_4$, $68h_5$ and $68h_2$ are provided with a logic "high", SCRs 62a, 61b, 63a and 62b are operated in a similar manner to that described above to connect the phases of the power supply 32 to the LIM primary 34 in the proper sequence so that the LIM primary 34 supplies the desired thrust to the vehicle. For a negative thrust, when conductors $68h_3$, $68h_5$ and $68h_2$ are provided with a logic "high", SCRs 65a, 61b, 64a and 65b are

operated in a similar manner to that described above to connect the phases of the power supply 32 to the LIM primary 34.

Once the SCRs become gated and the LIM primary 34 receives the supply voltage from the three phase power supply 32, the reaction rail 24 on the vehicle 16 completes the circuit with the LIM primary 34 and the vehicle 16 is provided with the proper thrust. As should be apparent, depending on the delay angle between the detected zero-crossing of the supply voltage and the operation of the SCRs as determined by the microcontroller, the amount of thrust generated by the LIM primary 34 is controlled. In this manner, the vehicle assumes the desired velocity V_d for it's position along the track as determined by the motion profile tables.

Figure 11 shows a block diagram of the motion control of a vehicle when travelling along the track through the control zones associates with three controllers 30. As can be seen, each controller 30 operates over a predetermined control zone and provides thrust to the vehicle 16 so that the vehicle assumes travel in accordance with the selected motion profile. Overlapping of control zones can occur so that more than one controller 30 provides thrust to the vehicle at a given time. This allows precision control of the vehicle along the track 12 to be achieved.

It should be apparent to one of skill in the art that various modifications can be made to the present system without departing from the scope thereof as defined by the appended claims.

We claim:

1. A velocity controller for a vehicle travelling along a path, said controller comprising:

sensing means disposed along said path at spaced intervals for detecting the presence of said vehicle, said sensing means generating output signals as said vehicle moves thereover;

processing means in communication with said sensing means, said processing means receiving said output signals and determining therefrom the velocity of said vehicle along said path;

memory means for storing at least one velocity profile representing the desired velocity of the vehicle along the path;

comparing means comparing the detected velocity of said vehicle with said velocity profile; and

velocity control means in communication with said comparing means, said velocity control means generating velocity correction signals to operate a linear motor driving said vehicle in a manner so that said vehicle assumes travel in accordance with said velocity profile when said detected velocity and said desired velocity are different.

2. A velocity controller as defined in Claim 1 wherein said sensing means includes a pair of spaced sensors, each of said sensors generating a sequence of output signals as a vehicle moves thereover, the sequence of said output signals determining the direction of travel of said vehicle moving along said path and the rate of change of said sequence determining the speed of the vehicle moving along said path.

3. A velocity controller as defined in Claim 2 wherein said processing means, memory means, comparing means and velocity control means are constituted by a microprocessor-based circuit.

4. A velocity controller as defined in Claim 3 wherein said memory means stores a plurality of velocity profiles therein, said comparing means selecting one of said velocity profiles as determined by predetermined operation control signals.

5. A velocity controller as defined in Claim 4 wherein said memory means is in communication with a host computer, said host computer downloading said velocity profiles to said memory means upon operation of said velocity controller.

6. A velocity controller as defined in Claim 5 further comprising velocity profile selecting means operable between a plurality of conditions to enable said comparing means to access one of said velocity profiles, said selecting switch means moving between said conditions in response to operation control signals generated by said host computer.

7. A velocity controller as defined in Claim 1 further comprising stop detection means in communication with said processing means for determining when said vehicle has stopped along said path in error, said stop detection means conditioning said velocity correction signals to a pre-determined value to ensure that said linear motor is operated in a manner to provide sufficient thrust to said vehicle to cause said vehicle to resume movement along said path in the desired direction.

8. A velocity controller as defined in Claim 1 further comprising jerk-limiting means in communication with said velocity control means, said jerk-limiting means comparing the difference between a velocity correction signal and a previously formed velocity correction signal with a pre-determined value, said jerk-limiting means allowing said velocity correction signal to pass to said linear motor when said difference is less than or equal to said pre-determined value and conditioning said velocity correction signal to a value equal to said pre-determined value when said difference is greater than said pre-determined value.

9. A velocity controller as defined in Claim 1 further comprising emergency stop logic in communication with said sensing means, said emergency stop logic operating said linear motor to cause said vehicle to stop upon detection of a sensing means failure.

10. A velocity controller as defined in Claim 9 wherein said emergency stop logic communicates with said processing means, said emergency stop logic operating said linear motor to cause said vehicle to stop when said vehicle is detected as travelling in an incorrect direction.

11. A velocity controller as defined in Claim 10 wherein said emergency stop logic operates said linear motor by generating a velocity correction signal having a magnitude and polarity to cause said linear motor to provide a reverse thrust to said vehicle and isolates said motor from velocity correction signals when said detected vehicle velocity is less than a pre-determined value.

12. A velocity controller as defined in Claim 1 further comprising vehicle position control means in communication with said processing means and said memory means, said position control means being operable when said vehicle is detected as being within a predetermined distance of a stopping point along said path as determined by said velocity profile, said position control means overriding said velocity control means upon operation thereof and generating said velocity correction signals to cause said vehicle to stop at said stopping point.

13. A velocity controller as defined in Claim 12 further including switch means operable between first and second conditions to connect one of said velocity or position control means to said linear motor, said switch means being biased to said first condition and being actuated to said second condition upon reception of switching signals generated by said position control means.

14. A velocity and position controller for controlling the movement of a vehicle along a path comprising:

sensing means disposed along said path at spaced intervals for detecting the presence of said vehicle, said sensing means generating output signals as said vehicle moves thereover;

processing means in communication with said sensing means, said processing means receiving said output signals and determining therefrom the velocity of said vehicle along said path;

memory means for storing at least one velocity profile representing the desired velocity of the vehicle along the path;

comparing means comparing the detected velocity of said vehicle with said velocity profile;

velocity control means in communication with said comparing means, said velocity control means generating velocity correction signals to operate a linear motor driving said vehicle in a manner so that said vehicle assumes travel in accordance with said velocity profile when said detected velocity and said desired velocity are different; and

vehicle position control means in communication with said processing means and said memory means, said position control means being operable when said vehicle is detected as being within a predetermined distance of a stopping point along said path, said position control means overriding said velocity control means upon operation thereof and generating said velocity correction signals to cause said vehicle to stop at said stopping point.

15. A velocity and position controller as defined in Claim 14 further including switch means operable between first and second conditions to connect one of said velocity and position control means to said linear motor, said switch means being biased to said first condition and being actuated to said second condition upon reception of switching signals generated by said position control means.

16. A velocity and position controller as defined in Claim 15 further comprising stop detection means in communication with said processing means for determining when said vehicle has stopped along said path in error, said stop detection means conditioning said velocity correction signals to a pre-determined value to ensure that said linear motor is operated in a manner to provide sufficient thrust to said vehicle

to cause said vehicle to resume movement along said path in the desired direction.

17. A velocity and position controller as defined in Claim 16 further comprising jerk-limiting means in communication with said switch means, said jerk-limiting means comparing the difference between a velocity correction signal and a previously formed velocity correction signal with a pre-determined value, said jerk-limiting means allowing said velocity correction signal to pass to said linear motor when said difference is less than or equal to a value equal to said pre-determined value and conditioning said velocity correction signal to a value equal to said pre-determined value when said difference is greater than said pre-determined value.

18. A velocity and position controller as defined in Claim 17 further comprising emergency stop logic in communication with said sensing means, said emergency stop logic operating said linear motor to cause said vehicle to stop upon detection of a sensing means failure.

19. A velocity and position controller as defined in Claim 18 wherein said emergency stop logic communicates with said processing means, said emergency stop logic operating said motor to cause said vehicle to stop when said vehicle is detected as travelling in an incorrect direction.

20. A velocity and position controller as defined in Claim 19 wherein said emergency stop logic operates said motor by generating a velocity correction signal having a magnitude and polarity to cause said

linear motor to provide a reverse thrust to said vehicle and isolates said motor from velocity correction signals when said detected vehicle velocity is less than a pre-determined value.

21. A transit system comprising:

a track for supporting a plurality of vehicles, each of said vehicles supporting a linear induction motor secondary and being of capable of travelling along said track;

linear induction motor primaries disposed along said track at spaced intervals, each of said primaries providing thrust to said vehicles within a control zone assigned thereto to propel said vehicles along said track;

a pair of sensors associated with each of said linear induction motor primaries and located on either side thereof, each of said sensors generating a sequence of output signals when a vehicle passes thereover;

a motor controller associated with each of said primaries and being in communication with each of said sensors associated with said primary, each of said motor controllers including processing means receiving said sequence of output signals from said sensors and determining therefrom the velocity of the vehicle travelling along said track;

memory means for storing at least one velocity profile representing the desired velocity of the vehicle along the track within said control zone;

comparing means comparing the detected direction of travel and speed of said vehicle with said velocity profile; and

velocity control means in communication with said comparing means, said velocity control means generating velocity

correction signals to operate said primary to cause said primary to supply thrust to said vehicle, said thrust being of a magnitude and direction so that said vehicle assumes travel along said track in accordance with said velocity profile.

22. A transit system as defined in Claim 21 wherein each controller further comprising vehicle position control means in communication with said processing means and said memory means, said position control means being operable when said vehicle is detected as being within a predetermined distance of a stopping point along said path, said position control means overriding said velocity control means upon operation thereof and generating said velocity correction signals to cause said vehicle to stop at said stopping point.

23. A transit system as defined in Claim 22 further including switch means operable between first and second conditions to connect one of said velocity or position control means to said primary, said switch means being biased to said first condition and being actuated to said second condition upon reception of switching signals generated by said position control means.

24. A transit system as defined in Claim 23 wherein said primaries are arranged along said track to enable more than one primary to supply thrust to a vehicle at a given time.

25. A transit system as defined in Claim 25 wherein said controllers remain inoperative until a sensor associated therewith detects the presence of a vehicle thereover.

26. A transit system as defined in Claim 25 further comprising a host computer connected to each of said controllers via a communication link, said host computer downloading said velocity profiles to each of said controllers upon power up of said system.

27. A three phase voltage controller to be connected between a three phase power supply and a linear motor primary comprising:

switching means operable between first and second conditions to connect and disconnect said primary to each phase of said power supply;

control means responsive to control signals for conditioning said switching means between said first and second conditions, said control means including sequencing means operable to condition said switching means to said first condition at a predetermined time to connect sequentially said primary to each phase of said power supply so that said primary receives a substantially identical supply voltage from each phase of said power supply at the time of connection thereto; and

delay means responsive to said control signals for inhibiting said sequencing means until said supply voltage reaches a desired level.

28. A controller as defined in Claim 27 wherein said switching means includes reversing means operable to reverse two of said three phases of said power supply to allow the direction of thrust output by said motor primary to be reversed.

29. A controller as defined in Claim 27 wherein said switching means is electrically isolated from said control means.

30. A controller as defined in Claim 27 wherein said sequencing means includes a shift register, said shift register being operable to output sequentially switching signals to said switching means upon the enabling thereof by said delay means.

31. A controller as defined in Claim 30 wherein said switching means comprises three pairs of silicon controlled rectifiers, each pair of said rectifiers being connected between one phase of said three phase power supply and said primary and being actuated to said first condition upon receipt of said switching signals.

32. A controller as defined in Claim 31 wherein said delay means includes a delay timer operable to delay shifting of said shift register until the voltage of said power supply attains said desired level, said control means further comprising a microprocessor-based circuit for analyzing an AC signal phased with one phase of said power supply and determining said delay based on the desired output of said primary, said microprocessor-based circuit setting said delay timer in response to said desired primary output, said delay timer enabling said shift register at a time equal to said delay after the first detected positive zero-crossing of said AC signal.

33. A controller as defined in Claim 32 wherein said switching means further comprises a transistor for each of said phases connected in series between a power source and a ground, said transistor receiving the output of said sequencing means on the base pin thereof and being operable to supply said rectifiers with said switching signal upon reception of the output signal of said sequencing means.

34. A controller as defined in Claim 33 wherein a transformer primary is also connected in series with said transistor, said transformer primary being in communication with a transformer secondary, said transformer secondary being energized upon energization of said transformer primary when said transistor is operational and supplying said switching signal to said rectifier.

35. A controller as defined in Claim 34 wherein said transformer secondary includes a rectifier circuit for rectifying said switching signal prior to being applied to said rectifier.

36. A controller as defined in Claim 27 further comprising interrupt means responsive to interrupt signals to isolate said power supply from said linear motor primary.

37. A controller as defined in Claim 36 wherein said interrupt means is in the form of a relay activated switch.

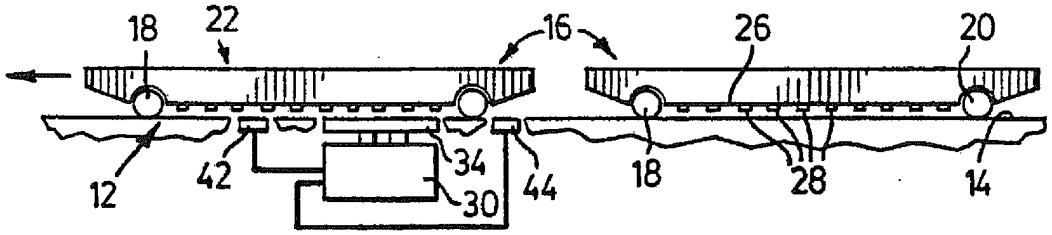

FIG.1a

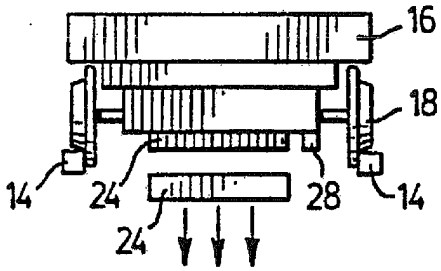

FIG.1b

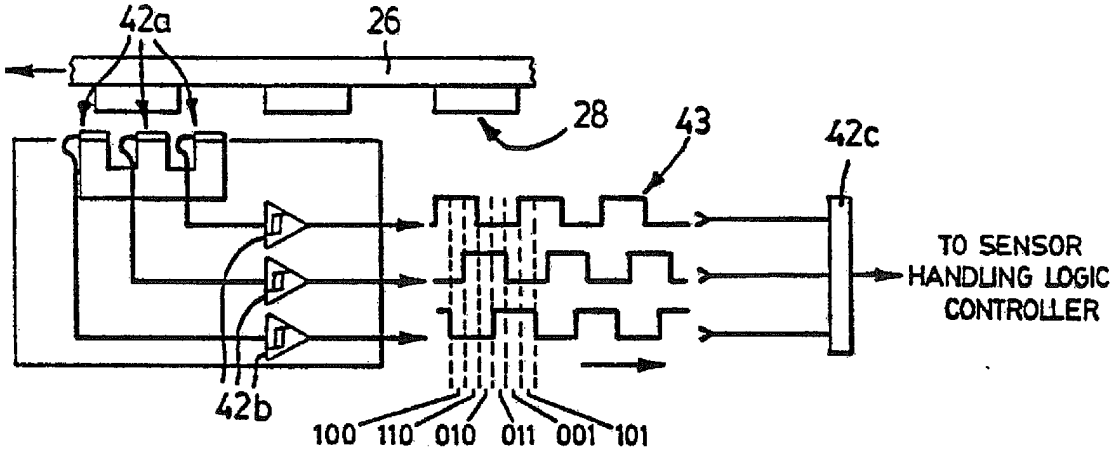

FIG.2

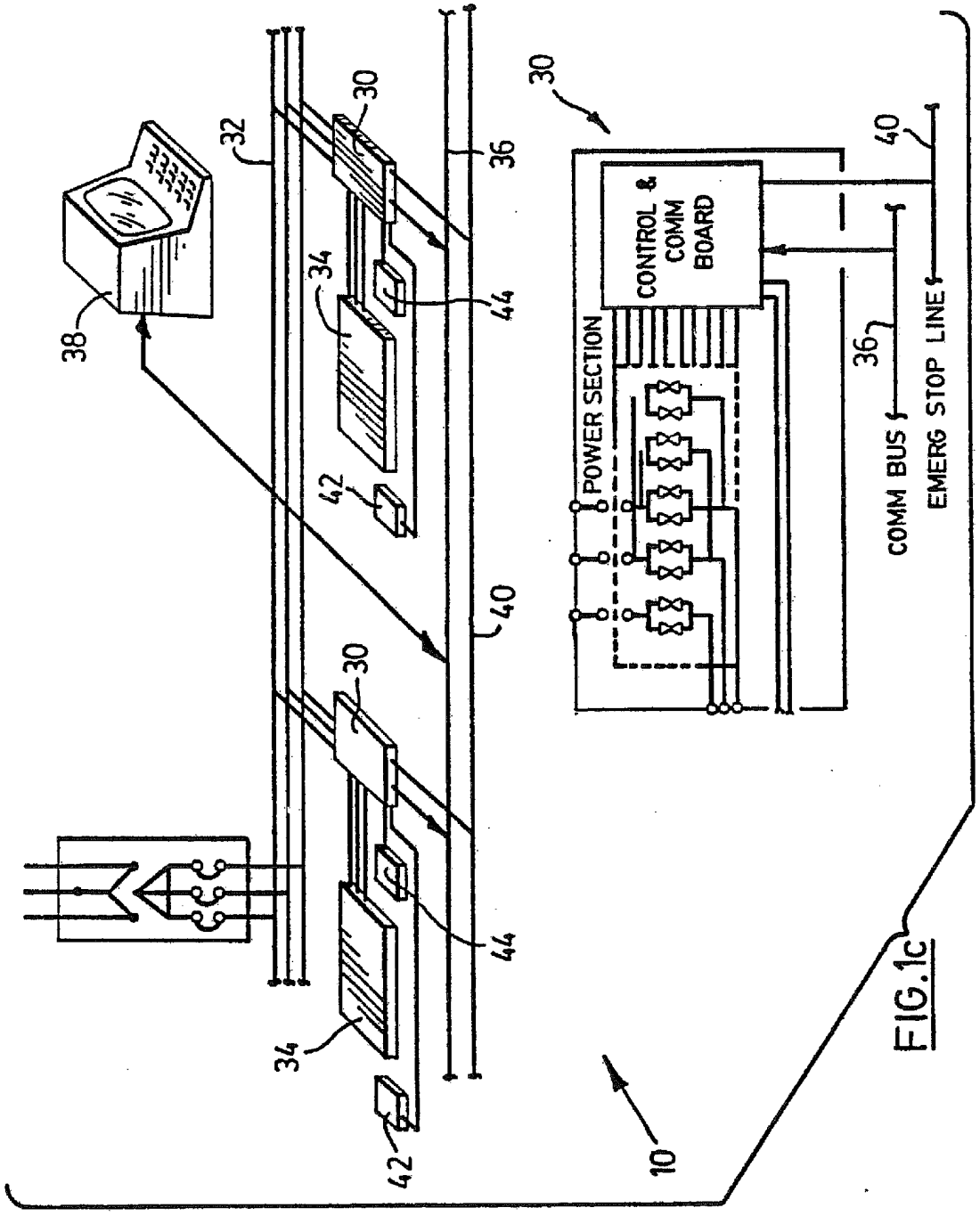
30
32
36
38
34
44
42
40
30
34
44
42
30
CONTROL & COMM BOARD
POWER SECTION
40
36
COMM BUS
EMERG STOP LINE
10

FIG. 1C

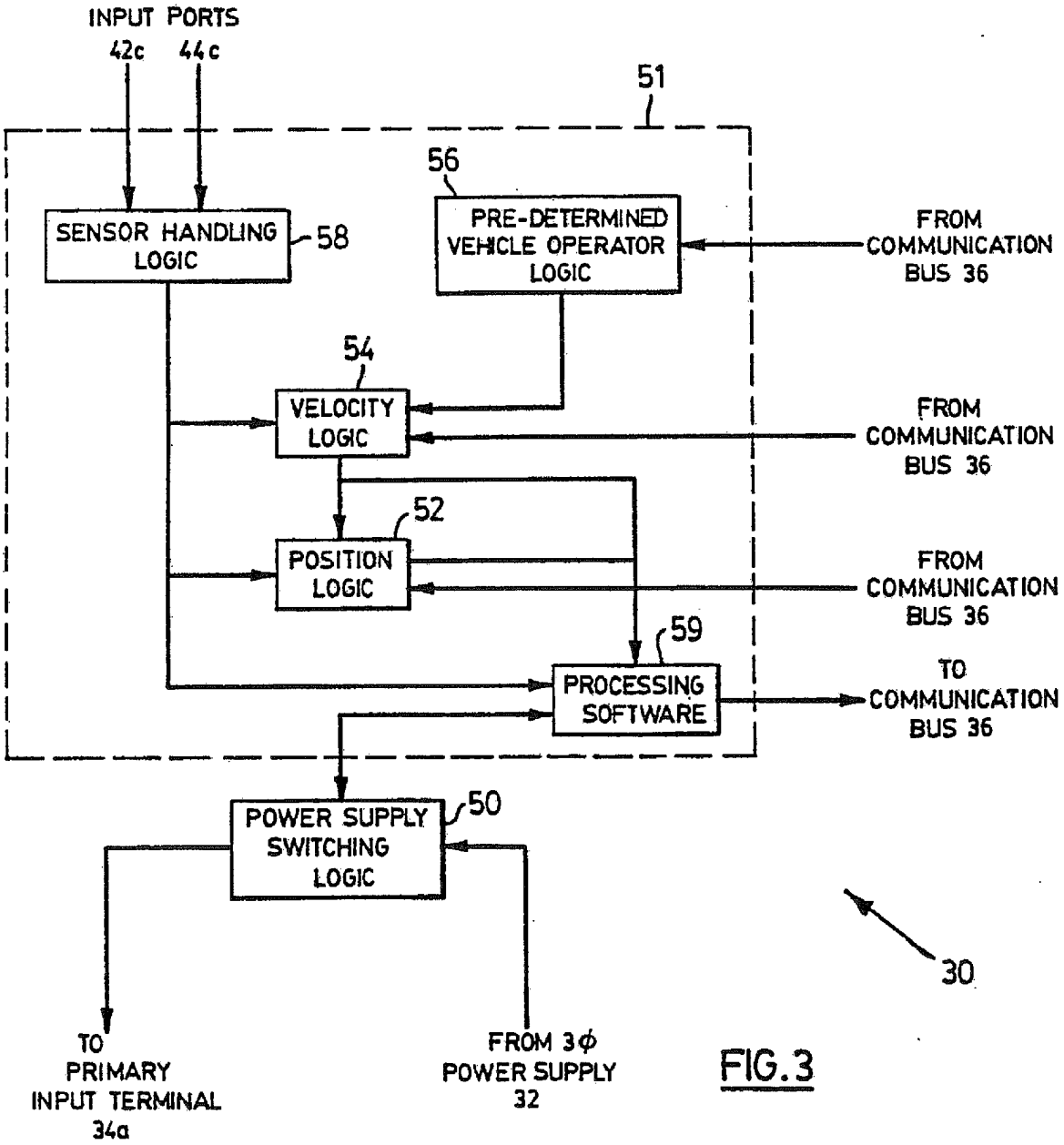
INPUT PORTS
42c
44c
51
56
SENSOR HANDLING LOGIC
58
PRE-DETERMINED VEHICLE OPERATOR LOGIC
FROM COMMUNICATION BUS 36
54
VELOCITY LOGIC
FROM COMMUNICATION BUS 36
52
POSITION LOGIC
FROM COMMUNICATION BUS 36
59
PROCESSING SOFTWARE
TO COMMUNICATION BUS 36
POWER SUPPLY SWITCHING LOGIC
50
30
TO PRIMARY INPUT TERMINAL 34a
FROM 3φ POWER SUPPLY 32

FIG.3

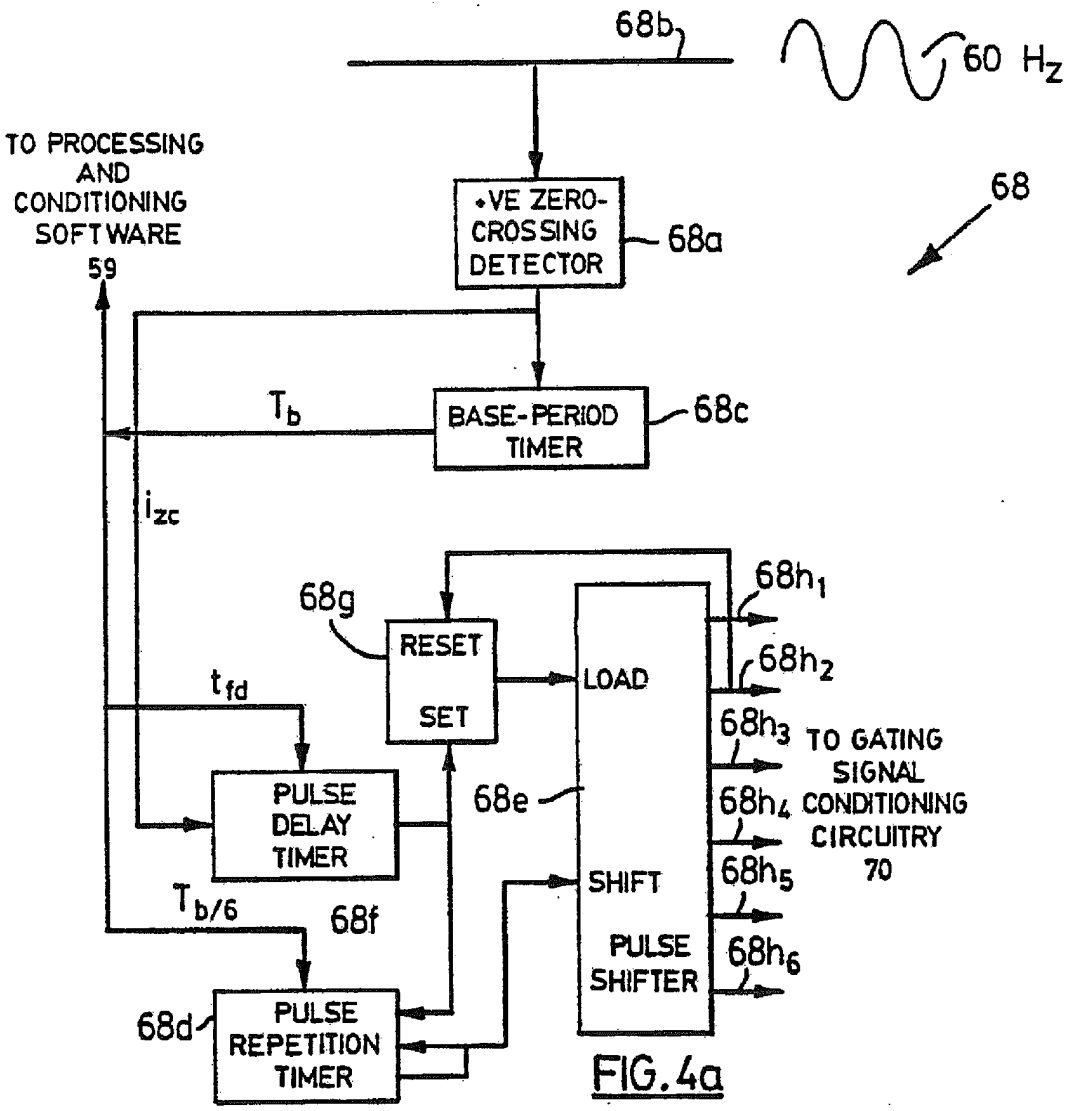
68b
60 Hz
TO PROCESSING AND CONDITIONING SOFTWARE 59
+VE ZERO-CROSSING DETECTOR
68a
68
T_b
BASE-PERIOD TIMER
68c
i_{zc}
68g
RESET
SET
t_{fd}
PULSE DELAY TIMER
68e
$T_{b/6}$
68f
68d
PULSE REPETITION TIMER
LOAD
SHIFT
PULSE SHIFTER
$68h_1$
$68h_2$
$68h_3$
$68h_4$
$68h_5$
$68h_6$
TO GATING SIGNAL CONDITIONING CIRCUITRY 70

FIG.4a

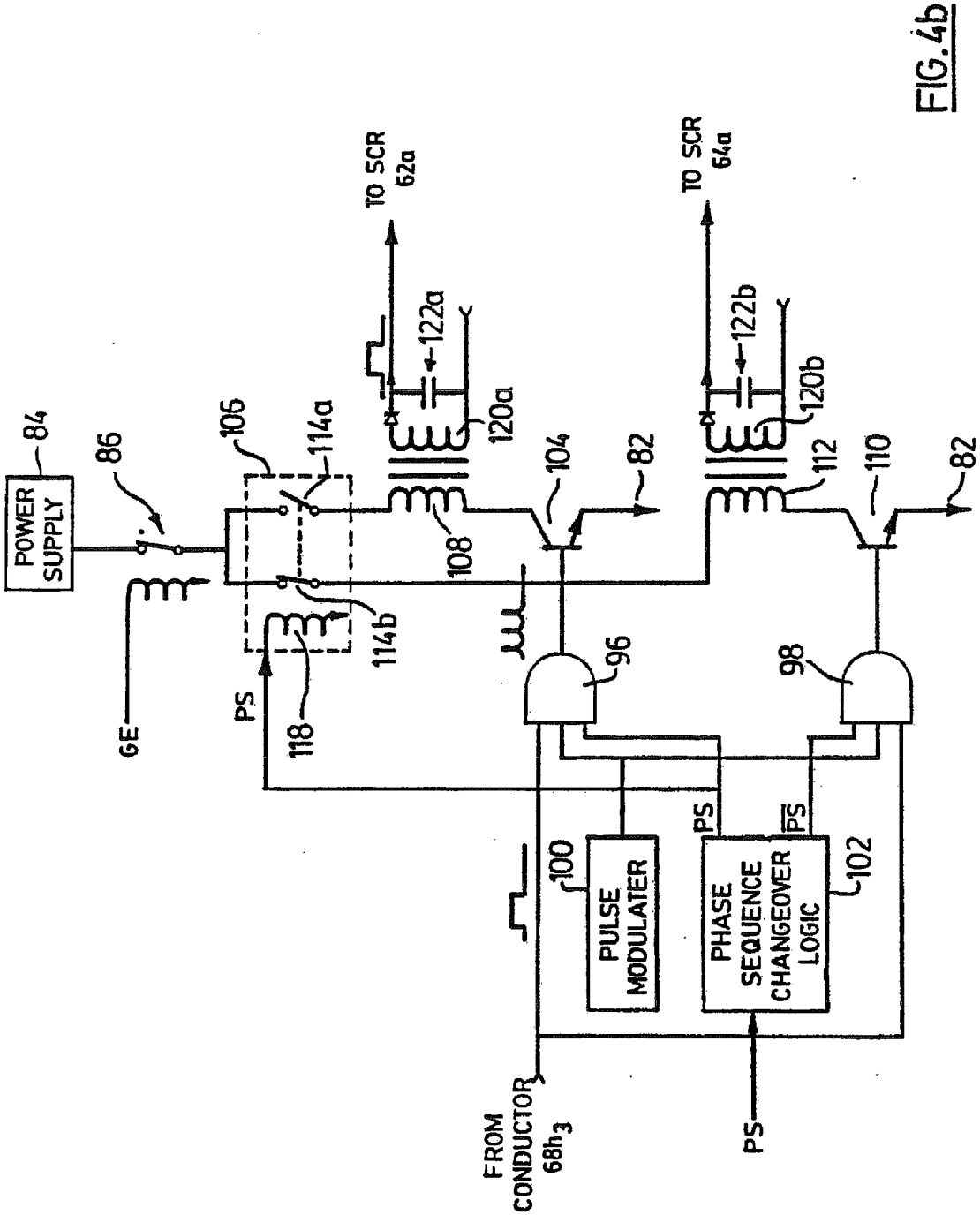
POWER SUPPLY
84
86
106
114a
114b
118
GE
PS
108
120a
122a
TO SCR 62a
104
82
120b
122b
TO SCR 64a
112
110
82
96
98
PS
PS
PS
100
PULSE MODULATER
PHASE SEQUENCE CHANGEOVER LOGIC
102
FROM CONDUCTOR 68h3

FIG.4b

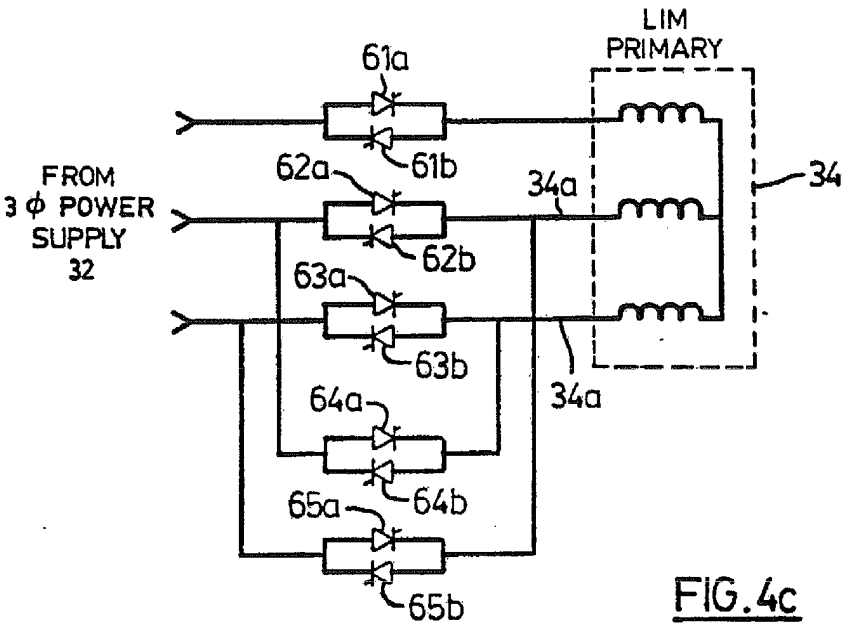
LIM
PRIMARY
61a
61b
62a
62b
63a
63b
64a
64b
65a
65b
FROM
3 ϕ POWER
SUPPLY
32
34
34a
34a

FIG.4c

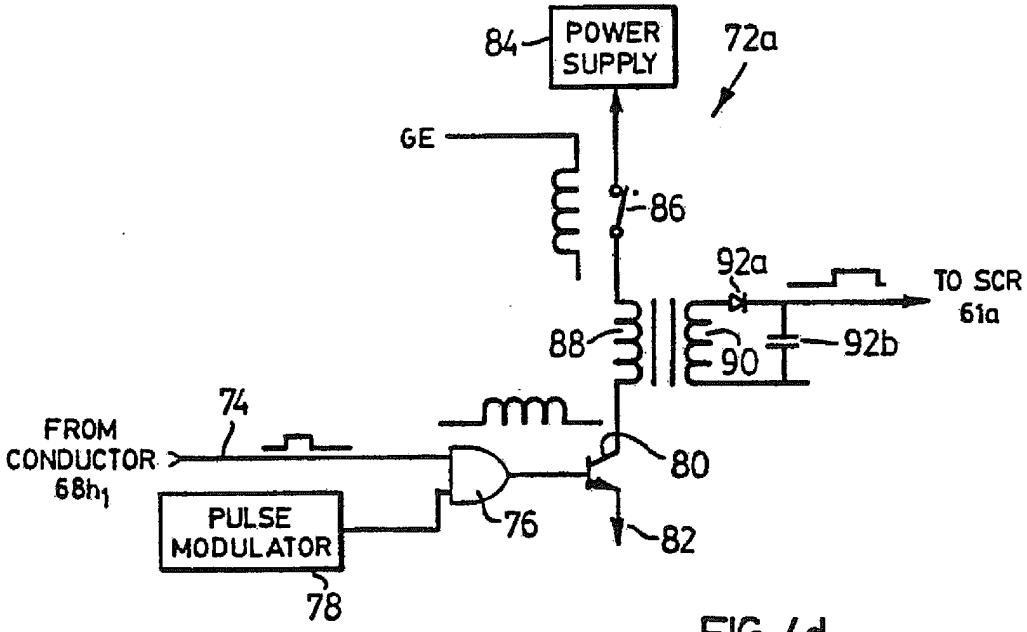
84
POWER
SUPPLY
72a
GE
86
92a
TO SCR
61a
88
90
92b
74
FROM
CONDUCTOR
68h1
80
PULSE
MODULATOR
76
82
78

FIG.4d

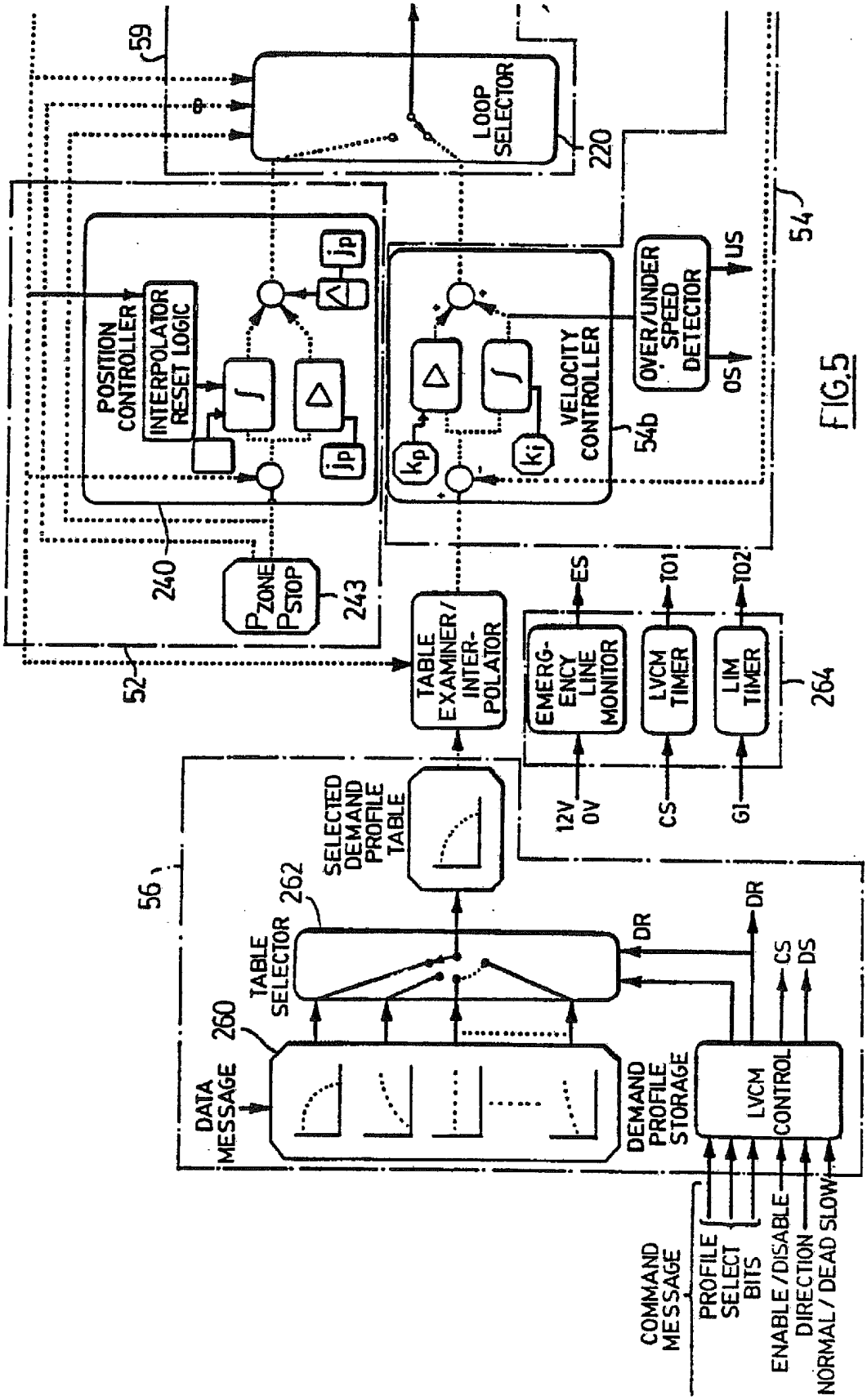
59
LOOP SELECTOR
220
54
POSITION CONTROLLER
INTERPOLATOR RESET LOGIC
VELOCITY CONTROLLER
54b
OVER/UNDER SPEED DETECTOR
US
OS
240
P ZONE
P STOP
243
52
TABLE EXAMINER/ INTER-POLATOR
EMERG-ENCY LINE MONITOR
ES
LVCM TIMER
T01
LIM TIMER
T02
264
12V
0V
CS
GI
56
SELECTED DEMAND PROFILE TABLE
262
TABLE SELECTOR
DR
260
DATA MESSAGE
DEMAND PROFILE STORAGE
LVCM CONTROL
CS
DS
COMMAND MESSAGE
PROFILE SELECT BITS
ENABLE/DISABLE
DIRECTION
NORMAL/DEAD SLOW

FIG.5

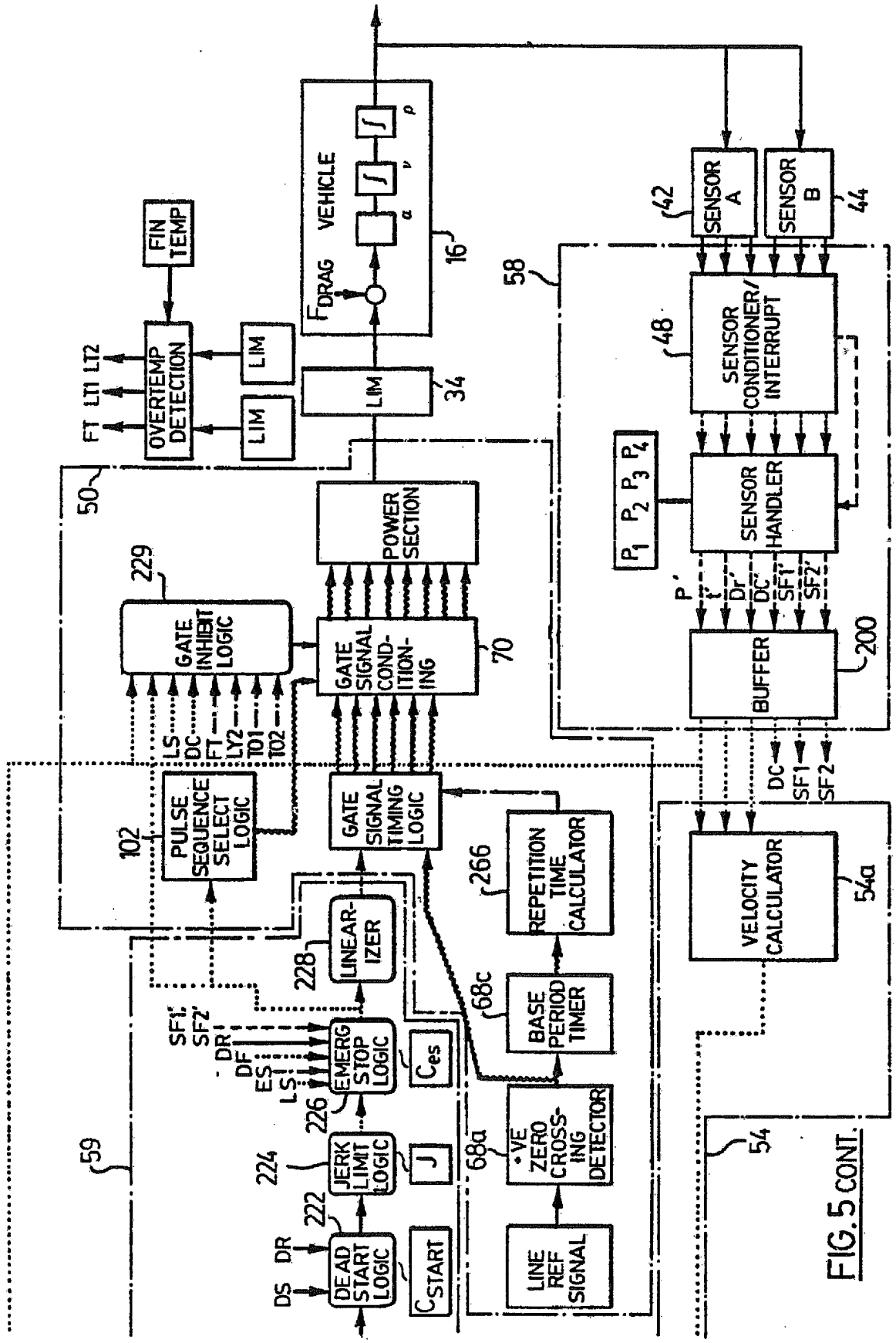
VEHICLE
F_{DRAG}
$\int$
a
v
ρ
16
FIN TEMP
OVERTEMP DETECTION
FT LT1 LT2
LIM
LIM
LIM
34
50
POWER SECTION
229
GATE INHIBIT LOGIC
GATE SIGNAL CONDITIONING
70
LS DC FT LY2 TO1 TO2
102
PULSE SEQUENCE SELECT LOGIC
GATE SIGNAL TIMING LOGIC
LINEARIZER
228
266
REPETITION TIME CALCULATOR
68c
BASE PERIOD TIMER
SF1' SF2' DR DF ES LS
EMERG STOP LOGIC
226
C_{es}
224
JERK LIMIT LOGIC
J
68a
VE ZERO CROSSING DETECTOR
222
DS DR
DEAD START LOGIC
C_{START}
LINE REF SIGNAL
59
58
42
SENSOR A
SENSOR B
44
48
SENSOR CONDITIONER/ INTERRUPT
P_1 P_2 P_3 P_4
SENSOR HANDLER
P' t' Dr' DC' SF1' SF2'
BUFFER
200
DC SF1 SF2
VELOCITY CALCULATOR
54a
54

FIG. 5 CONT.

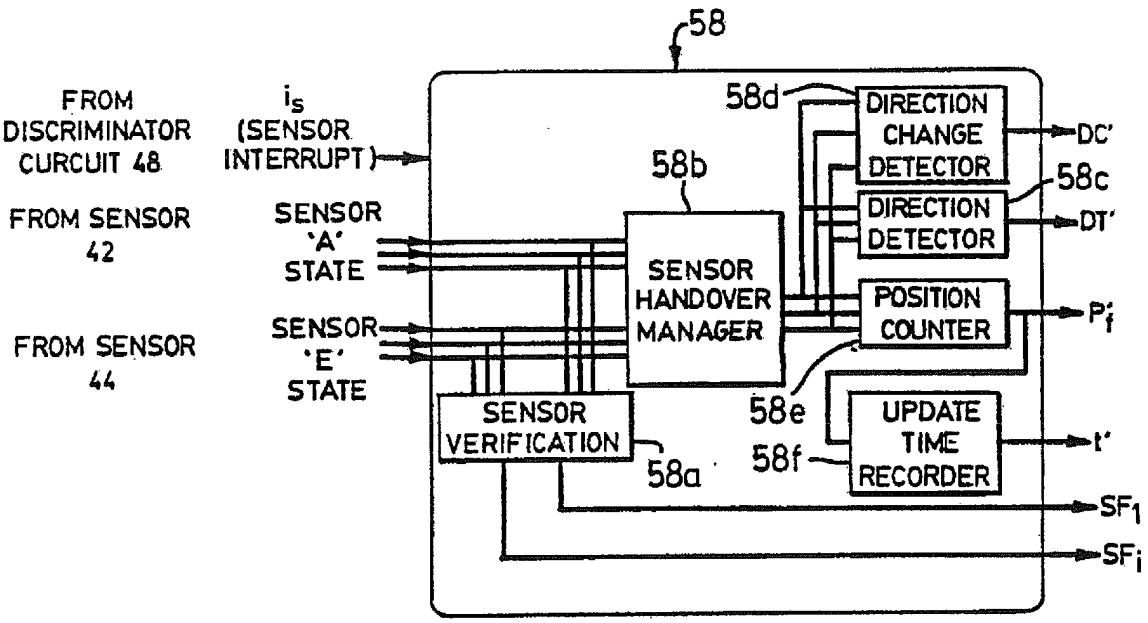
58
FROM DISCRIMINATOR CURCUIT 48
i_s (SENSOR INTERRUPT)
FROM SENSOR 42
SENSOR 'A' STATE
FROM SENSOR 44
SENSOR 'E' STATE
58b
SENSOR HANDOVER MANAGER
58d
DIRECTION CHANGE DETECTOR
DC'
58c
DIRECTION DETECTOR
DT'
POSITION COUNTER
P_f'
SENSOR VERIFICATION
58a
58e
58f
UPDATE TIME RECORDER
t'
SF_1
SF_i

FIG. 6

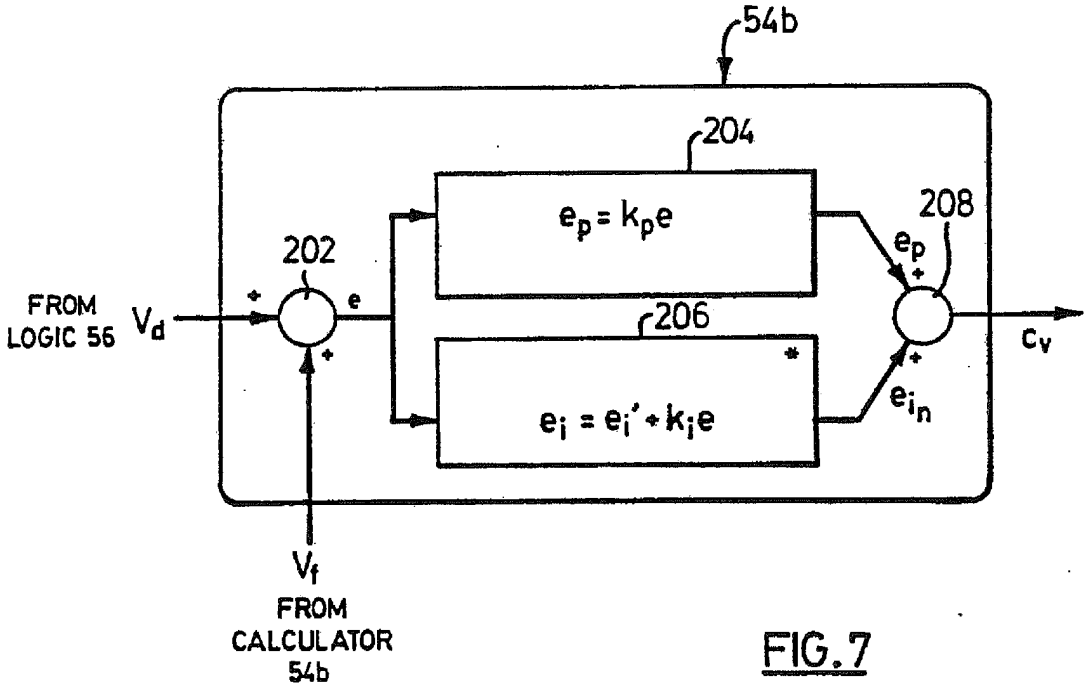
54b
204
$e_p = k_p e$
208
e_p
202
FROM LOGIC 56
V_d
e
206
$e_i = e_i' + k_i e$
e_{i_n}
c_v
V_f
FROM CALCULATOR 54b

FIG. 7

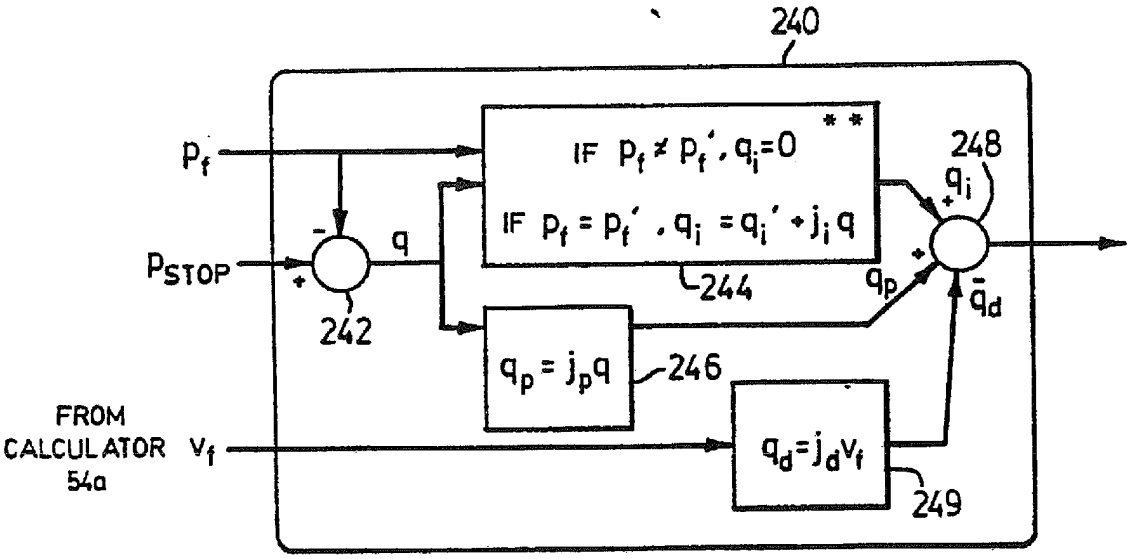
240
P_f
P_{STOP}
q
242
IF $P_f \neq P_f'$, $q_i=0$ **
IF $P_f = P_f'$, $q_i = q_i' + j_i q$
244
248
q_i
q_p
$\bar{q}_d$
$q_p = j_p q$
246
FROM CALCULATOR 54a
V_f
$q_d = j_d V_f$
249

FIG. 8

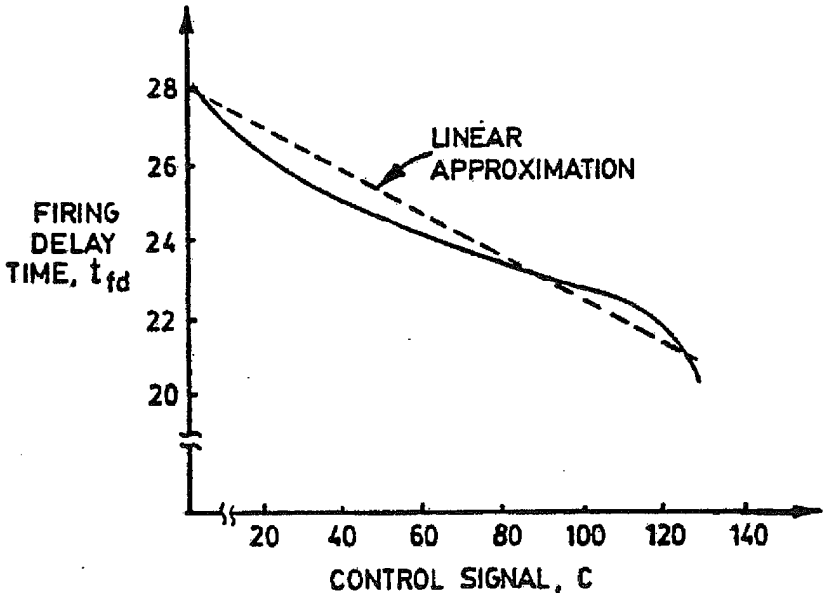
28
26
24
22
20
FIRING DELAY TIME, t_{fd}
LINEAR APPROXIMATION
20
40
60
80
100
120
140
CONTROL SIGNAL, C

FIG. 9

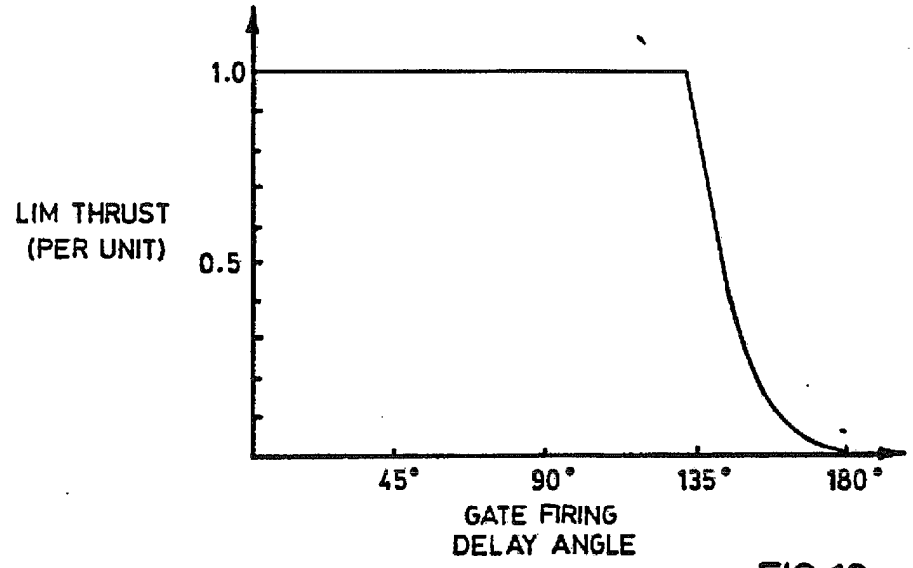
1.0
0.5
LIM THRUST
(PER UNIT)
45°
90°
135°
180°
GATE FIRING
DELAY ANGLE

FIG.10

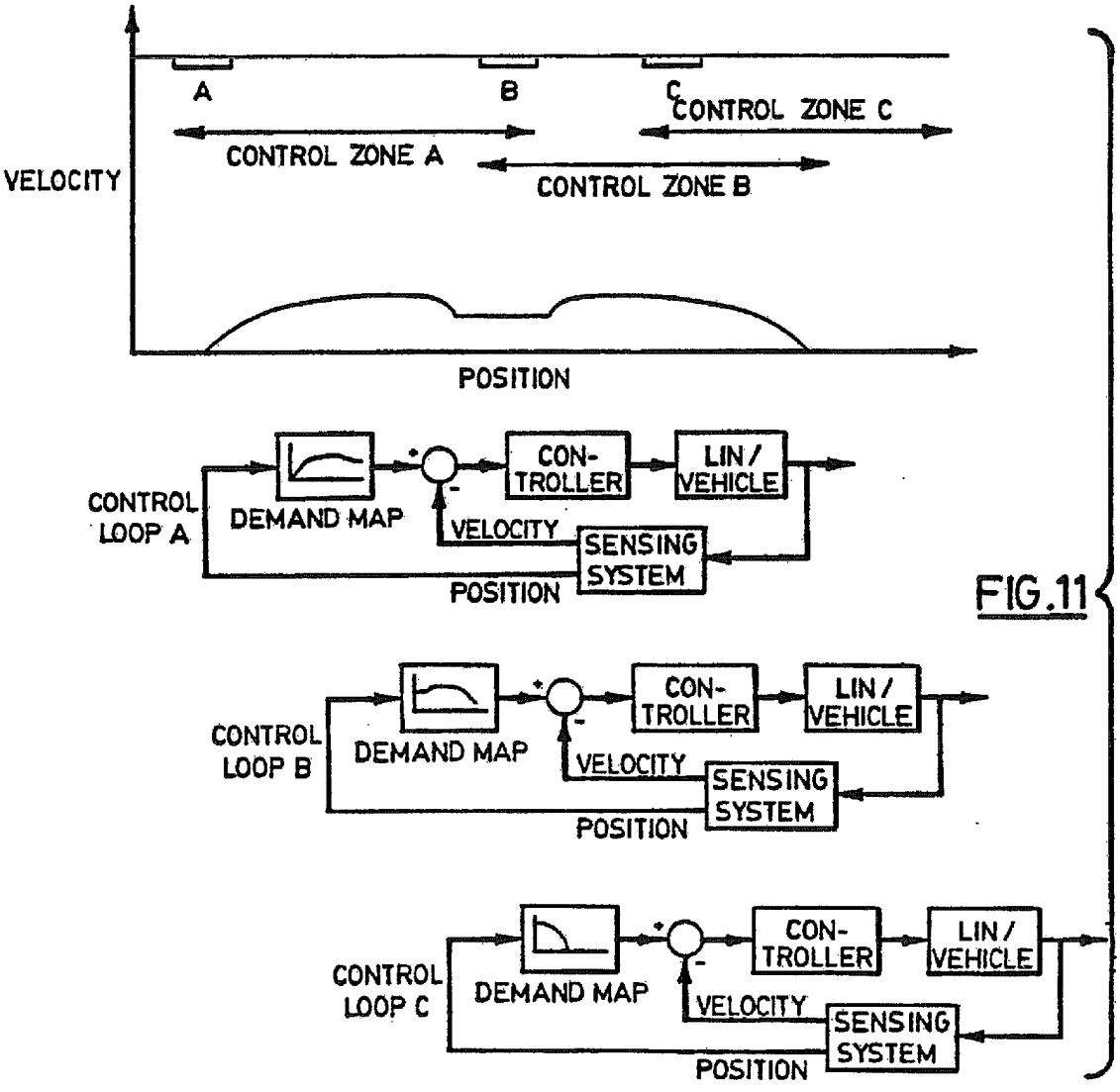
A
B
C
CONTROL ZONE C
CONTROL ZONE A
CONTROL ZONE B
VELOCITY
POSITION
CONTROL LOOP A
DEMAND MAP
CON-TROLLER
LIN / VEHICLE
VELOCITY
SENSING SYSTEM
POSITION
CONTROL LOOP B
DEMAND MAP
CON-TROLLER
LIN / VEHICLE
VELOCITY
SENSING SYSTEM
POSITION
CONTROL LOOP C
DEMAND MAP
CON-TROLLER
LIN / VEHICLE
VELOCITY
SENSING SYSTEM
POSITION

FIG.11

INTERNATIONAL SEARCH REPORT

International Application No PCT/CA 90/00461

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 B60L15/00

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	B60L ; H02K

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	US,A,3803466 (R.C. STARKEY) 09 April 1974 see abstract; figures 5, 10	1
A		3, 9, 14, 18, 21, 27
A	US,A,4675582 (W.J. HOMMES ET AL) 23 June 1987 see abstract; figures 1, 5, 8	1-6, 14, 21, 26, 27, 31
A	US,A,3974778 (M.G. BLACK ET AL) 17 August 1976 see abstract; figures 1, 6	1, 14, 21, 27
A	EP,A,188657 (CHRYSLER CORP.) 30 July 1986 see abstract; figures 1, 3	1-6, 14, 21, 27
A	EP,A,294541 (MAGNET-BAHN GMBH) 14 December 1988 see abstract; figures 6, 7, 13, 14	27-33

-/--

[9] Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
25 MARCH 1991	19. 04. 91
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	BEYER F.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,4777420 (H. DADPEY ET AL) 11 October 1988 see figure 7 ---	1, 8, 17

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. CA9000461

SA 42990

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 25/03/91
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-3803466	09-04-74	None		
US-A-4675582	23-06-87	AU-B-	593378	08-02-90
		AU-A-	7803387	19-01-89
		EP-A-	0321473	28-06-89
		WO-A-	8810531	29-12-88
		US-A-	4853602	01-08-89
US-A-3974778	17-08-76	None		
EP-A-188657	30-07-86	US-A-	4633148	30-12-86
		JP-A-	61173607	05-08-86
EP-A-294541	14-12-88	DE-A-	3176678	07-04-88
		EP-A,B	0052343	26-05-82
		EP-A-	0052344	26-05-82
		EP-A,B	0052345	26-05-82
		EP-A,B	0052346	26-05-82
		EP-A-	0216202	01-04-87
		EP-A-	0300123	25-01-89
		EP-A-	0300124	25-01-89
		EP-A-	0299137	18-01-89
		EP-A-	0315727	17-05-89
		EP-A-	0300125	25-01-89
		EP-A-	0301164	01-02-89
		EP-A-	0300126	25-01-89
		EP-A-	0298194	11-01-89
		EP-A-	0278532	17-08-88
US-A-4777420	11-10-88	None		